# Classification of Amplifiers

| Type of Signal | Based on No.of Stages | Type of Configuration | Classification based on conduction angle | Frequency of Operation |
|---|---|---|---|---|
| Small Signal | Single Stage | Common Emitter | Class A Amplifier | Direct Current (DC) |
| Large Signal | Multistage | Common Base | Class B Amplifier | Audio Frequencies (AF) |
| | | Common Collector | Class AB Amplifier | Radio Frequencies (RF) |
| | | | Class C Amplifier | VHF, UHF and SHF Frequencies |

# Different Regions Of Operation

| Region of Operation | Emitter Base Junction | Collector Base Junction |
|---|---|---|
| Cut off | Reverse biased | Reverse biased |
| Active | Forward biased | Reverse biased |
| Saturation | Forward biased | Forward biased |

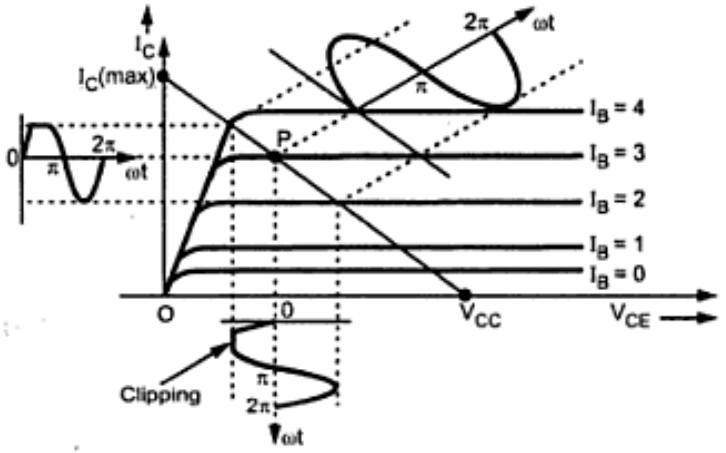
# Transistor Voltage specifications For Various Operating Regions

| Transistor | $V_{CE\,(sat)}$ | $V_{BE\,(sat)}$ | $V_{BE\,(active)}$ | $V_{BE\,(cut\text{-}in)}$ | $V_{BE\,(cut\text{-}off)}$ |
|---|---|---|---|---|---|
| Si | 0.2 V | 0.8 V | 0.7 V | 0.5 V | 0 V |
| Ge | 0.1 V | 0.3 V | 0.2 V | 0.1 V | – 0.1 V |

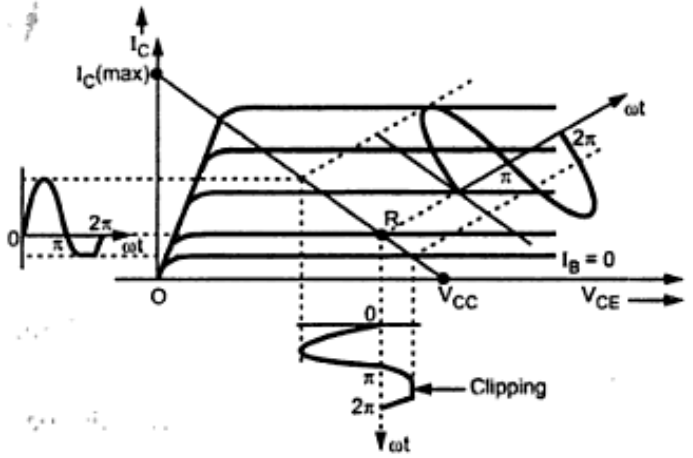
# Condition for Active & Saturation Regions

**For saturation :** $$I_B > \frac{I_C}{\beta_{dc}}$$

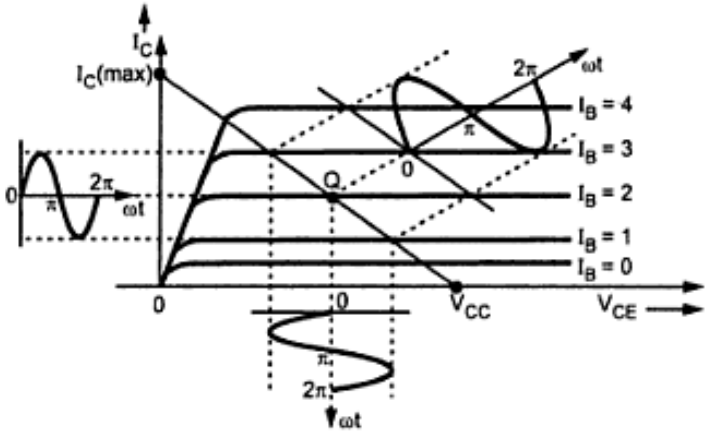
**For active region :** $$V_{CE} > V_{CE\,(sat)}$$




**Operating point near saturation region gives clipping at the positive peaks**

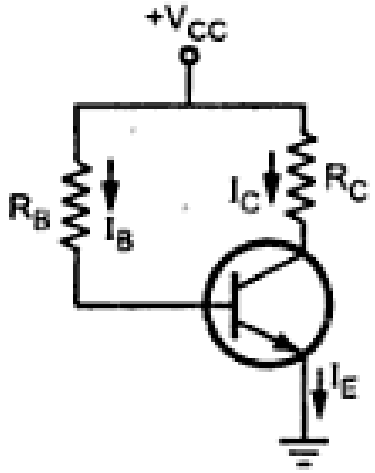



**Operating point near cut-off region gives clipping at the negative peaks**

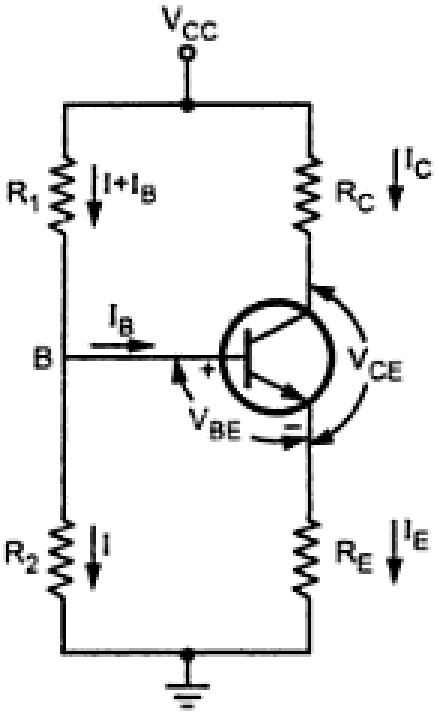



**Operating point at the centre of active region is most suitable**

# Transistor Biasing

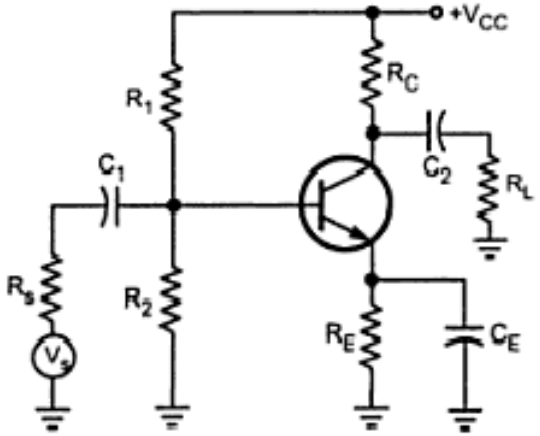



Fixed bias circuit

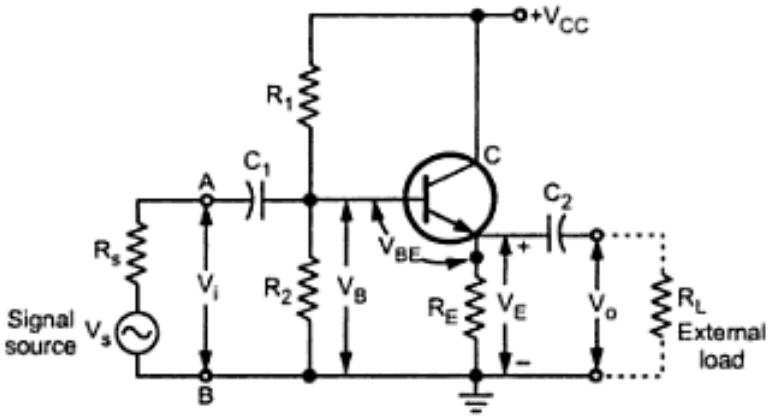



Voltage divider bias circuit

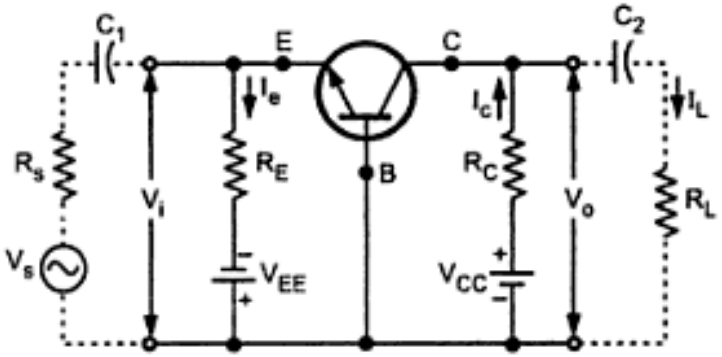
# CE, CC, & CB Amplifiers




Practical common emitter amplifier circuit




Common collector circuit




Common base circuit

# H-Parameters Representation Of An Amplifier


$$V_i = h_{11} I_i + h_{12} V_o$$
$$I_o = h_{21} I_i + h_{22} V_o$$

**Definitions of h-parameter**

The parameters in the above equation are defined as follows :

$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}$ = Input resistance with output short-circuited, in ohms.

$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}$ = Fraction of output voltage at input with input open circuited.

This parameter is ratio of similar quantities, hence unitless

$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$ = Forward current transfer ratio or current gain with output short circuited.

This parameter is a ratio of similar quantities, hence unitless.

$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}$ = Output admittance with input open-circuited, in mhos.

**a) With output short circuited :**

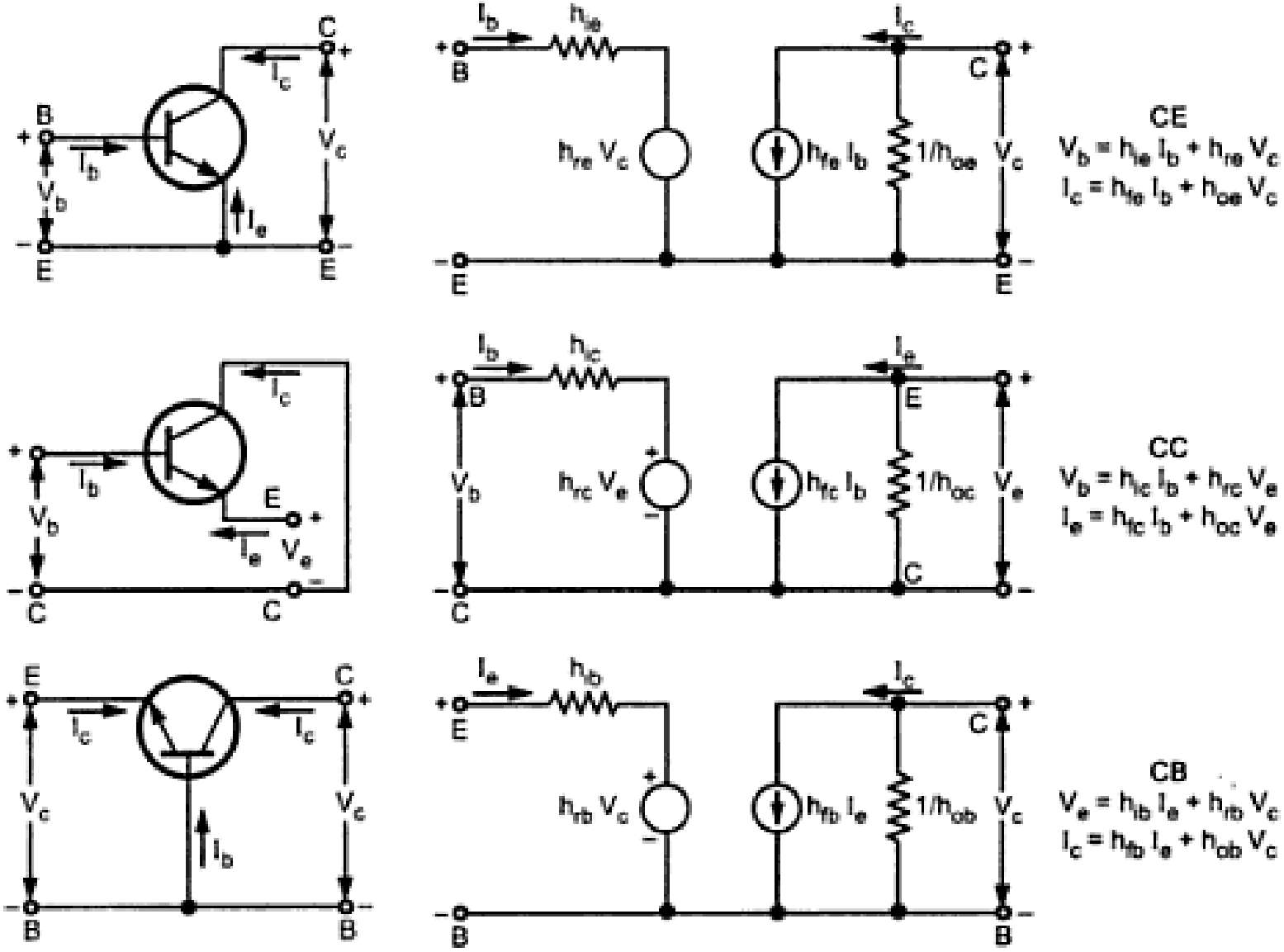
$h_{11} = h_i$ : Input resistance

$h_{21} = h_f$ : Short circuit current gain

**b) With input open circuited :**

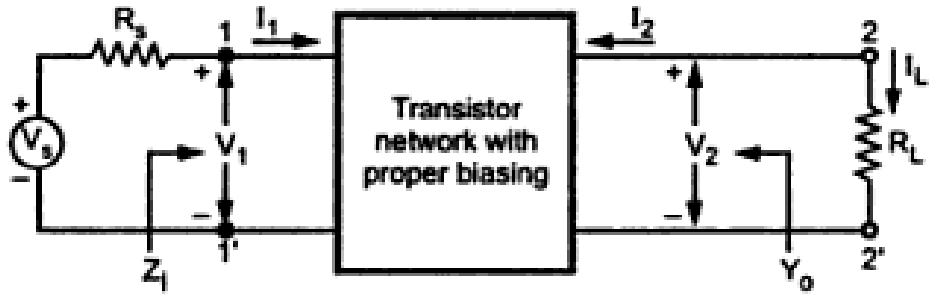
$h_{12} = h_r$ : Reverse voltage transfer ratio

$h_{22} = h_o$ : Output admittance

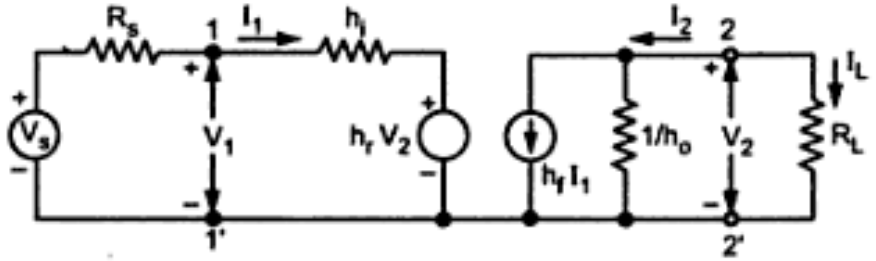



**Transistor configurations and their hybrid models**

# Small Signal Analysis Of A Junction Transistor




**Basic transistor amplifier**




**Transistor amplifier in its h-parameter model**

small-signal analysis of a transistor amplifier

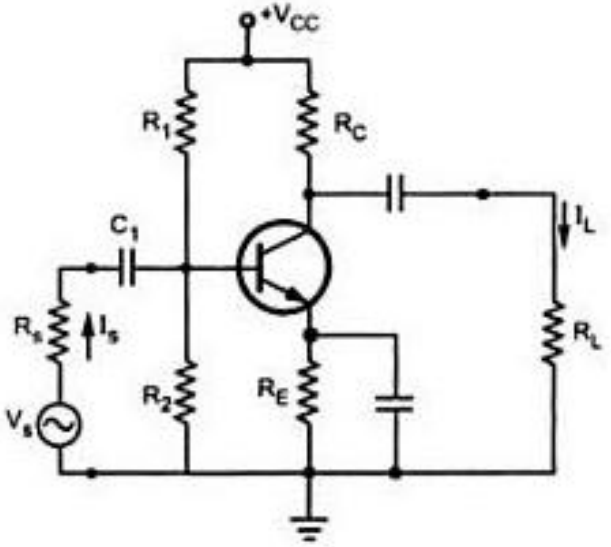
| |
|---|
| $A_i = -\dfrac{h_f}{1 + h_o R_L}$ |
| $A_{is} = \dfrac{A_i R_s}{Z_i + R_s}$ |
| $Z_i = h_i + h_r A_i R_L = h_i - \dfrac{h_f h_r}{h_o + Y_L}$ |
| $A_v = \dfrac{A_i R_L}{Z_i}$ |
| $A_{VS} = \dfrac{A_v R_i}{Z_i + R_s} = \dfrac{A_i R_L}{Z_i + R_s} = \dfrac{A_{is} R_L}{R_s}$ |
| $Y_o = h_o - \dfrac{h_f h_r}{h_i + R_s} = \dfrac{1}{Z_o}$ |
| $A_P = A_V A_i = A_i^2 \dfrac{R_L}{Z_i}$ |

# Guidelines for Analysis of a Transistor Circuit

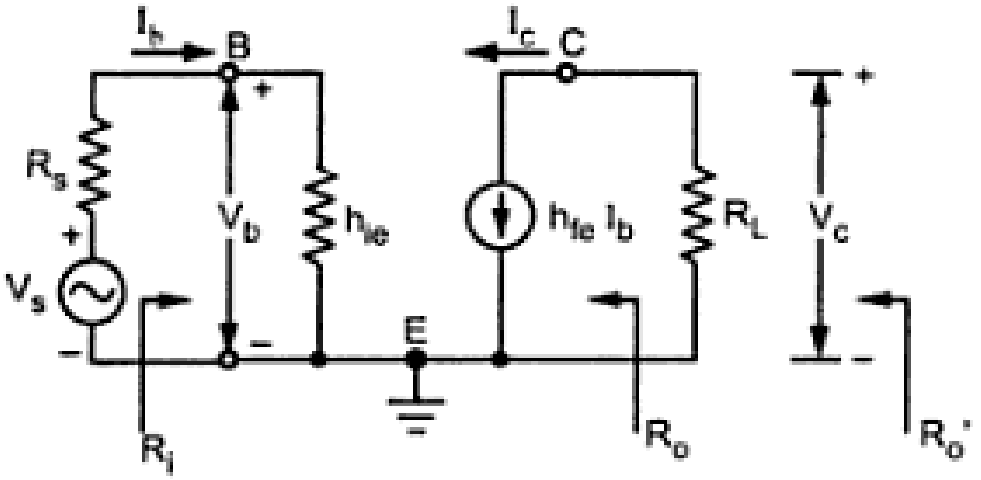
1. Draw the actual circuit diagram.
2. Replace coupling capacitors and emitter bypass capacitor by short circuit.
3. Replace dc source by a short circuit. In other words, short $V_{CC}$ and ground lines.
4. Mark the points B(base), C(collector), E(emitter) on the circuit diagram and locate these points as the start of the equivalent circuit.
5. Replace the transistor by its h-parameter model.

# Design Problem

➡ *Consider a single stage CE amplifier with* $R_s = 1\ k\Omega$, $R_1 = 50\ K$, $R_2 = 2K$, $R_C = 1K$, $R_L = 1.2\ K$, $h_{fe} = 50$, $h_{ie} = 1.1\ K$, $h_{oe} = 25\ \mu A/V$ *and* $h_{re} = 2.5\times10^{-4}$, *as shown in Fig.*



# Approximate H-Model For CE Amplifier




Approximate CE model

**Current Gain** $A_i \approx -h_{fe}$

**Input Impedance** $R_i \approx h_{ie}$

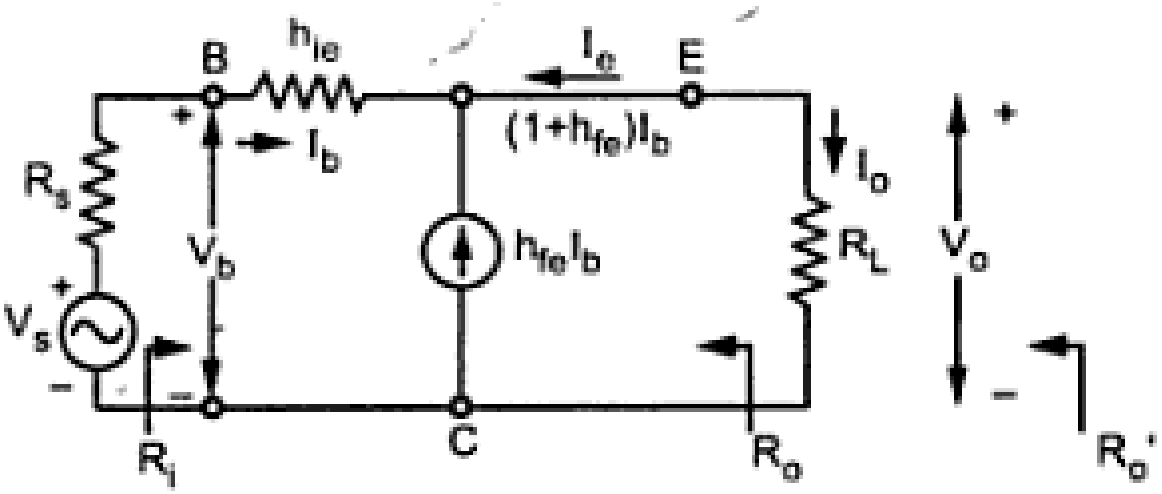
**Voltage Gain :** $A_v = \frac{A_i R_L}{R_i} = \frac{A_i R_L}{h_{ie}}$

**Output Impedance** $Y_o = 0$

$R_o = \frac{1}{Y_o} = \infty$

$R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L$

# Approximate H-Model For CC Amplifier




**Simplified CC model**

**Current gain** $A_i = \frac{I_o}{I_b} = \frac{-I_e}{I_b} = 1 + h_{fe}$

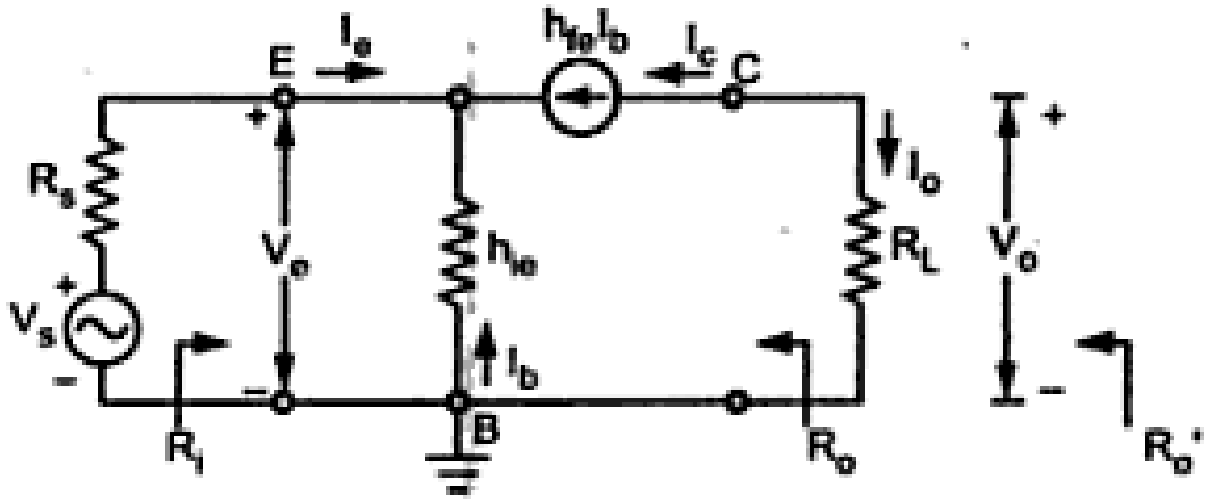
**Input resistance :** $R_i = \frac{V_b}{I_b} = h_{ie} + (1 + h_{fe})\, R_L$

**Voltage gain ($A_v$)** $A_v = \frac{(1 + h_{fe}) R_L}{h_{ie} + (1 + h_{fe}) R_L} \cong 1$

**Output resistance $R_o$** $R_o = \frac{V_o}{I_e} = \frac{R_s + h_{ie}}{1 + h_{fe}}$

$$R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L$$

# Approximate H-Model For CB Amplifier




**Simplified CB model**

**Current gain** $A_i = \dfrac{h_{fe}}{1 + h_{fe}}$

**Input resistance ($R_i$)** $R_i = \dfrac{h_{ie}}{1 + h_{fe}}$

**Voltage gain ($A_v$)** $A_v = \dfrac{\dfrac{h_{fe}}{1 + h_{fe}} \times R_L}{\dfrac{h_{ie}}{1 + h_{fe}}} = \dfrac{h_{fe} R_L}{h_{ie}}$

**Output resistance ($R_o$)** $R_o = \left.\dfrac{V_o}{I_c}\right|_{V_s = 0}$

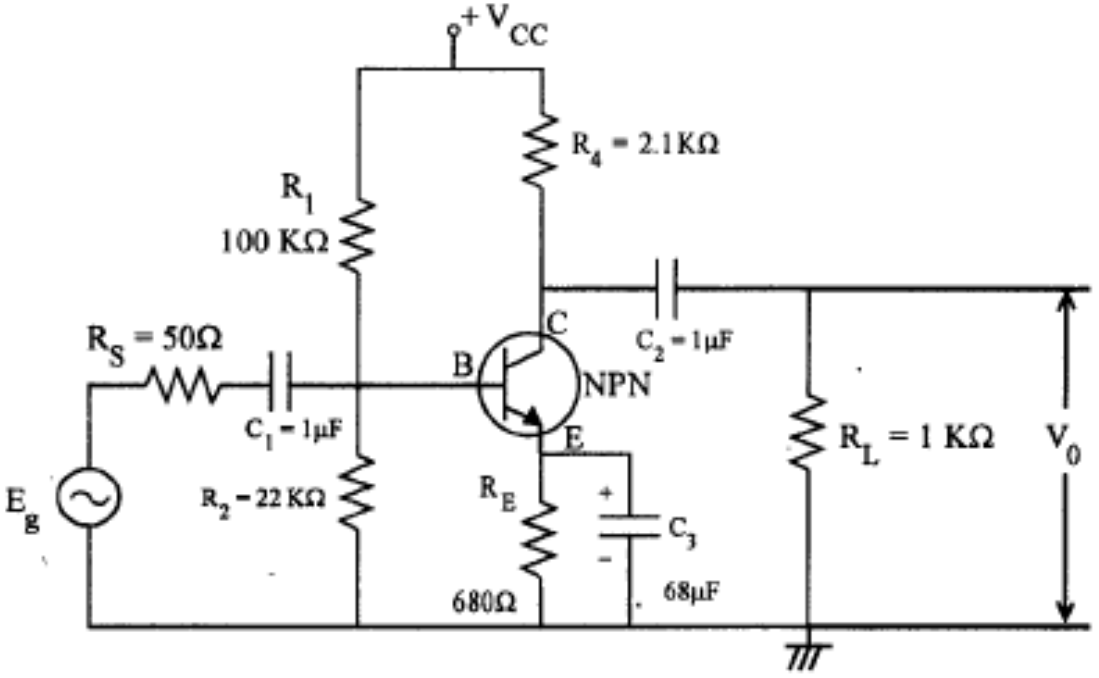
$$R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L$$

# Design Problem

For the circuit shown in Fig. estimate $A_i$, $A_v$, $R_i$ and $R_o$ using reasonable approximations. The ***h-parameters*** for the transistor are given as

$h_{fe} = 100$ $h_{ie} = 2000\ \Omega$ $h_{re}$ is negligible and $h_{oe} = 10^{-5}$ mhos(℧).

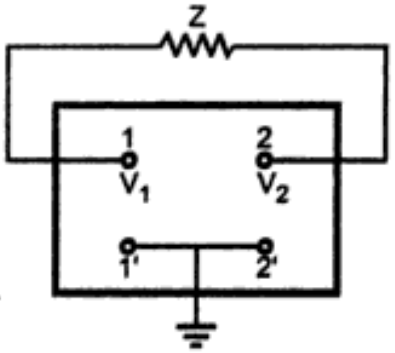
$I_b = 100\ \mu A$.



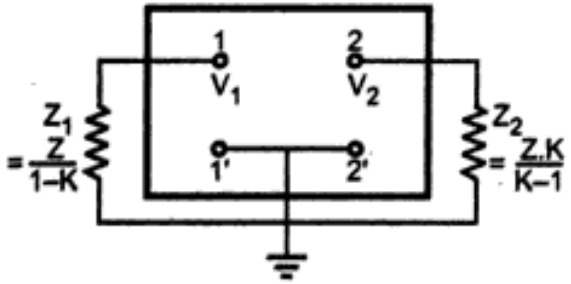

CE Amplifier Circuit

# Miller's Theorem

**Millers theorem is used to simplify the analysis of a circuit whenever there is a feedback connection in the circuit**




(a)

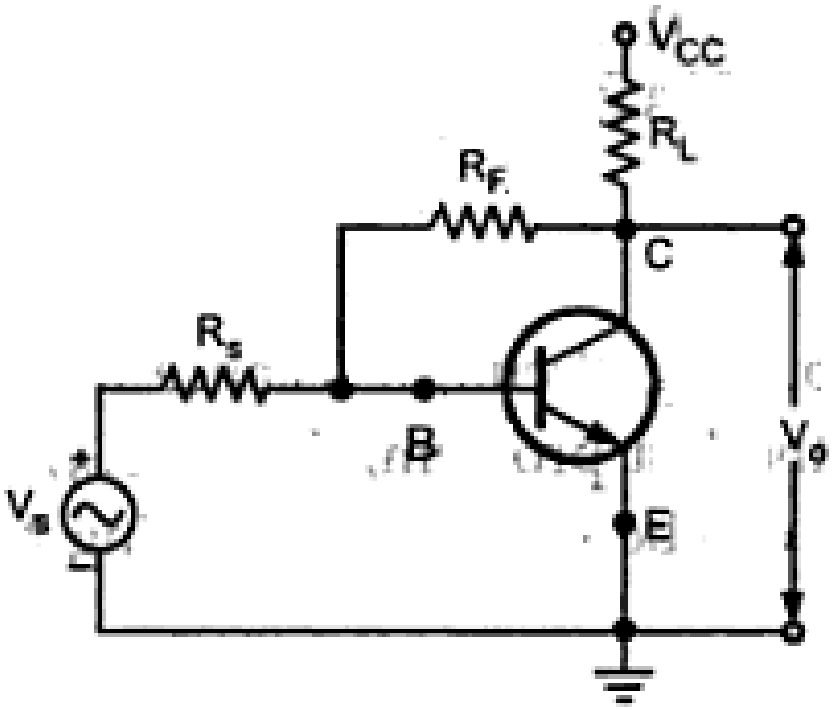



(b)

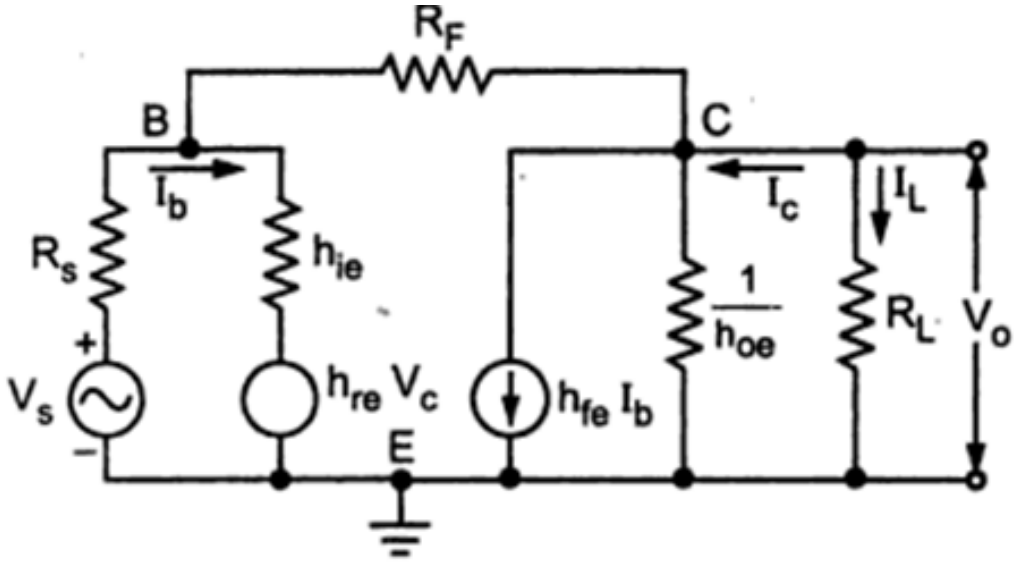
$$Z_1 = \frac{Z}{1-K}$$

$$Z_2 = \frac{Z \cdot K}{K-1}$$

# Analysis of Common Emitter Amplifier with Collector to Base Bias

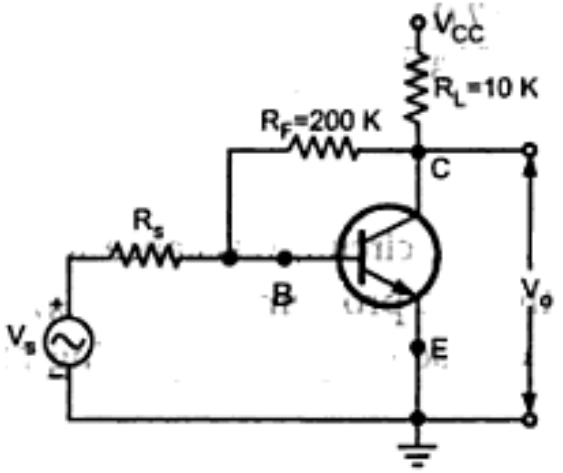


# AC equivalent circuit



# Design Problems

➠ *The Fig. shows common emitter amplifier with collector to base bias. Calculate $R_i$, $R_i'$, $A_v$, $A_{vs}$, $A_i$. The transistor parameters are $h_{ie} = 1.1$ K, $h_{fe} = 50$, $h_{oe} = 25 \times 10^{-6}$ A/V, $h_{re} = 2.5 \times 10^{-4}$.*



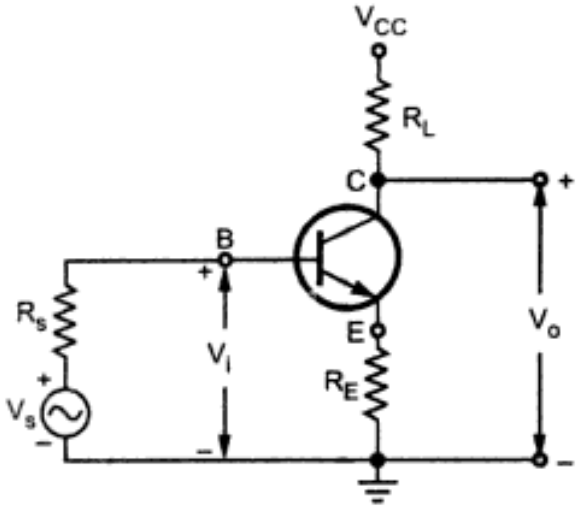
# Design Problems

➠ For a Common Emitter Configuration, what is the maximum value of $R_L$ for which $R_1$ differs by not more than 10% of its value at $R_2 = 0$ ?

$h_{ie} = 1100\Omega$ ; $h_{fe} = 50$

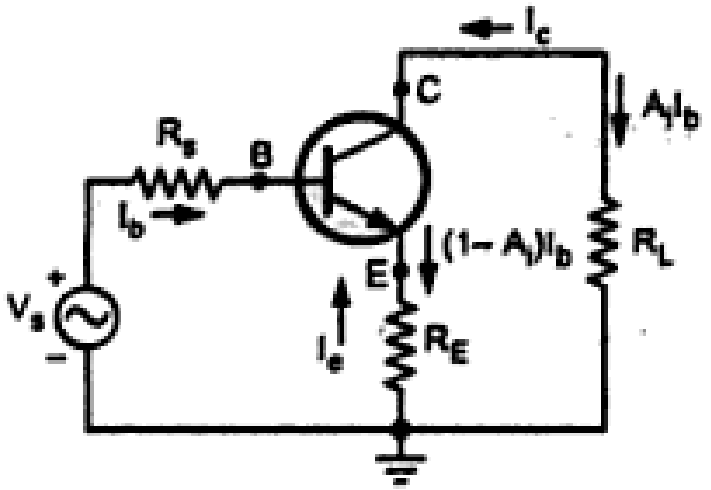
$h_{re} = 2.50 \times 10^{-4}$ ; $h_{oe} = 25\mu$ A/v

# Analysis Of CE Amplifier With Unbypassed $R_E$

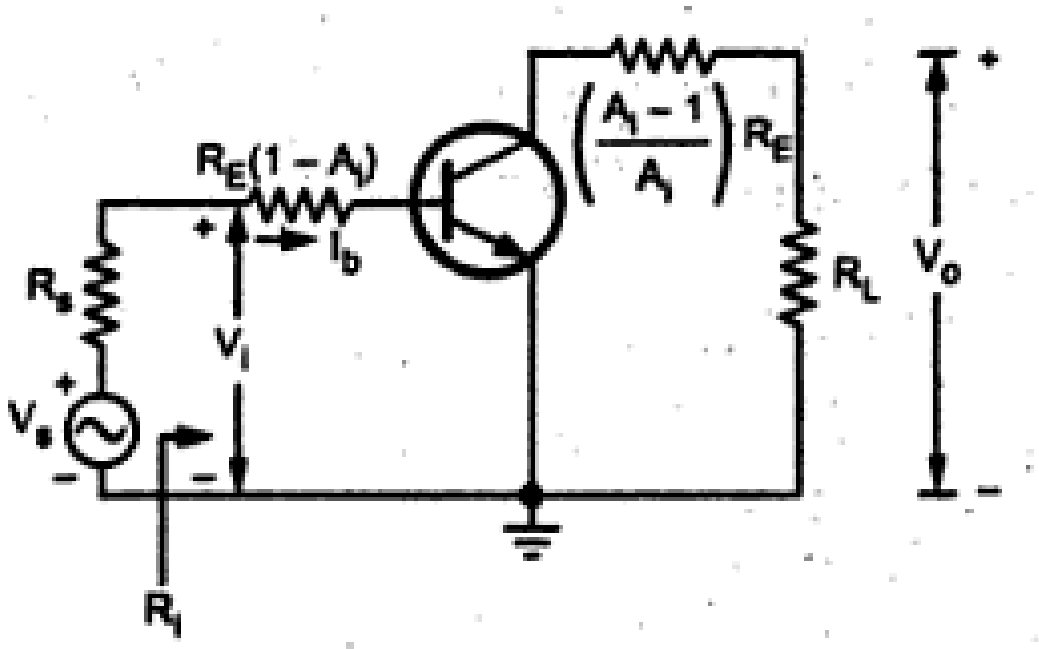



- $R_E$ is added to stabilize the gain of the amplifier
- $R_E$ acts as a feedback resistor
- The overall gain will reduce with unbypassed $R_E$

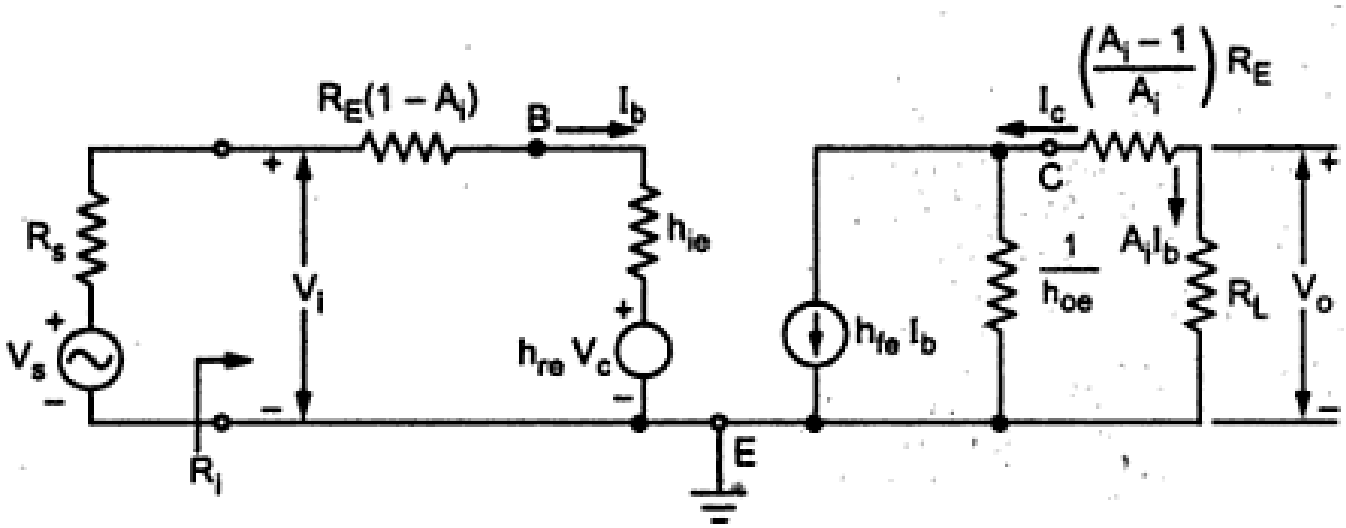
# AC Equivalent Circuit For CE Amplifier with Unbypassed $R_E$



# AC Equivalent Circuit For CE Amplifier with $R_E$ Splitted using dual of Miller's Theorem

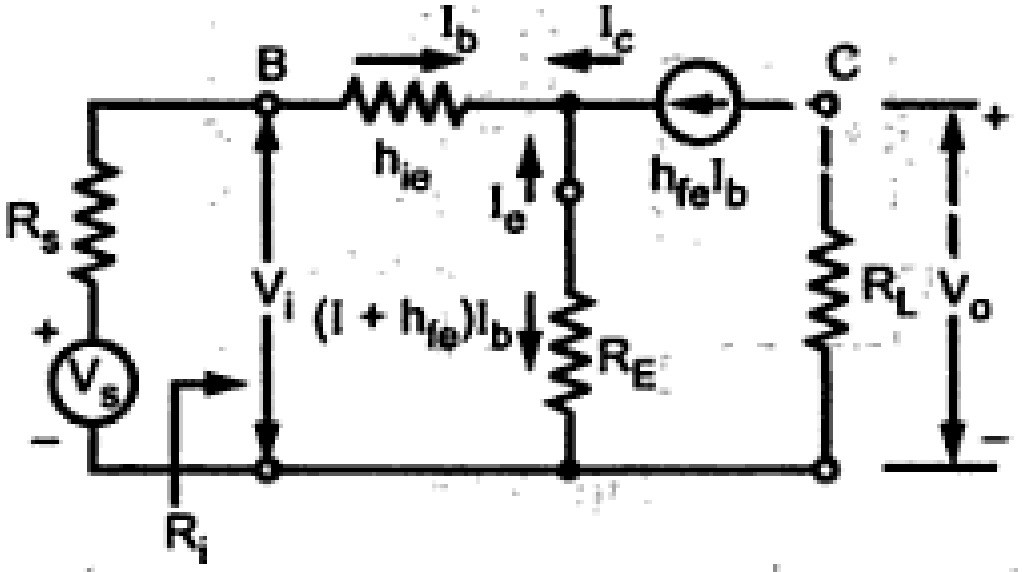


# h-Parameter Equivalent Circuit (Exact Analysis)




$$A_i = \frac{-h_{fe}}{1 + h_{oe} R'_L} = \frac{-h_{fe}}{1 + h_{oe}\left(R_L + \frac{A_i - 1}{A_i} R_E\right)}$$

# h-Parameter Equivalent Circuit (Approximate Analysis)




**Approximate model for CE amplifier with $R_E$**

**Current gain** $A_i = \dfrac{-I_c}{I_b} = \dfrac{-h_{fe} I_b}{I_b} = -h_{fe}$

**Input resistance** $R_i = \dfrac{V_i}{I_b} = h_{ie} + (1 + h_{fe})\, R_E$

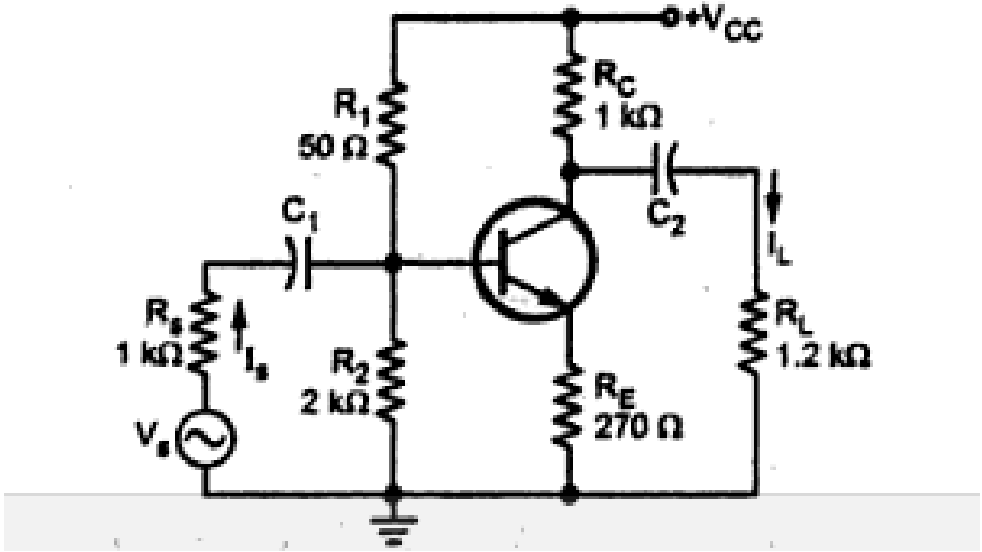
**Voltage gain** $A_v = \dfrac{A_i R_L}{R_i} = \dfrac{-h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_E}$

**Output resistance** $R_o = \left.\dfrac{V_o}{I_o}\right|_{V_s = 0}$

$R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L$

# Design Problems

➠ **Example** *Fig. shows a single stage CE amplifier with unbypassed emitter resistance find current gain, input resistance, voltage gain and output resistance. Use typical values of h-parameter*

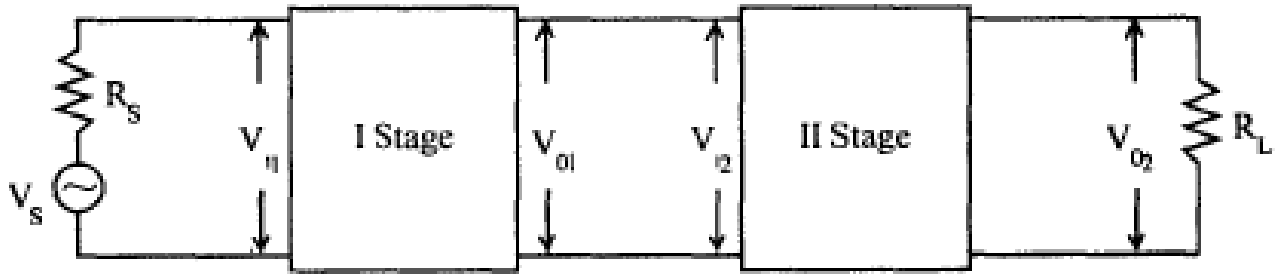


# MULTISTAGE AMPLIFIERS

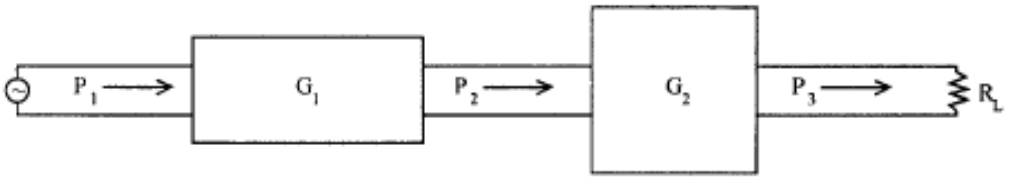
# Need For Cascading

- When the amplification of a single stage amplifier is not sufficient, or,
- When the input or output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected, in cascade. Such amplifier, with two or more stages is also known as multistage amplifier.

# Block diagram of 2-Stage Cascade Amplifier




# Gain of 2-Stage Cascade Amplifier



$$G_1 = \frac{P_2}{P_1}; \quad G_2 = \frac{P_3}{P_2}$$

Overall gain $$G = \frac{P_3}{P_1}$$

$$= \frac{P_2}{P_1} \cdot \frac{P_3}{P_2}$$

$$G = G_1 G_2$$

## Decibel Voltage Gain

### Cascaded Stages

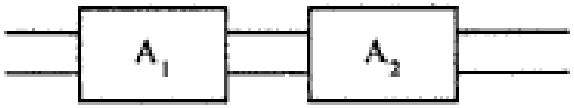



**Fig. 2.23** Cascaded stages

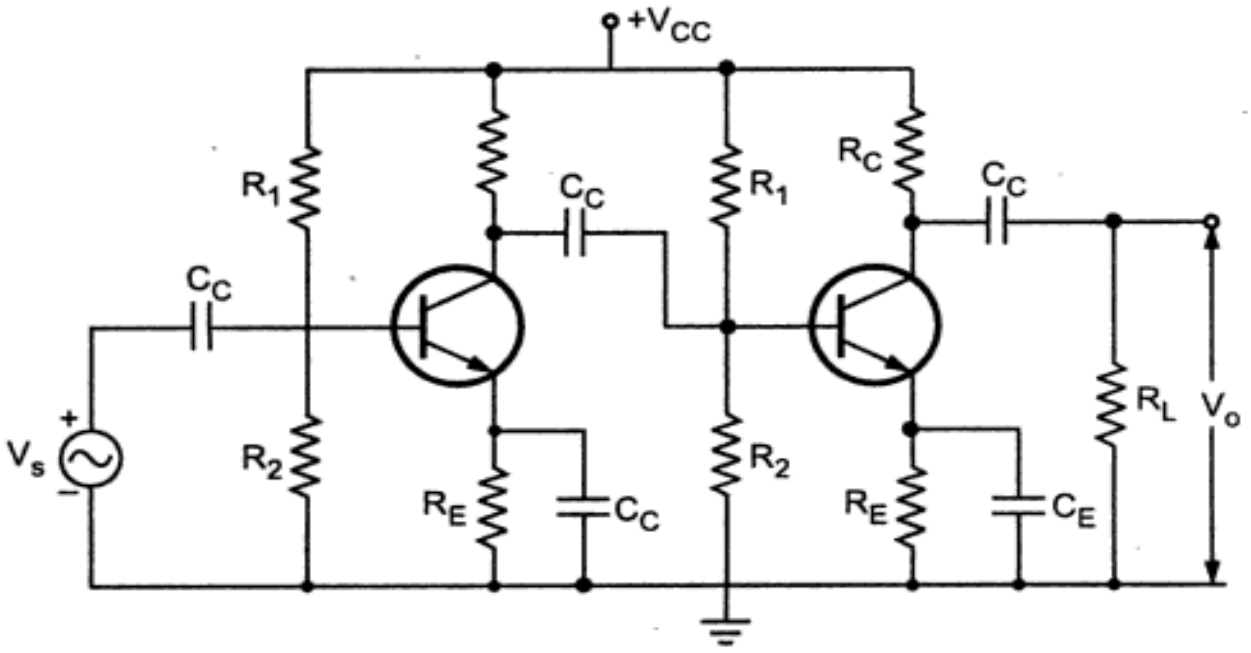
$$A = A_1 \times A_2$$

$$A_1 = A_1' + A_2' \text{ (in decibels)}$$

## Methods of Inter Stage Coupling

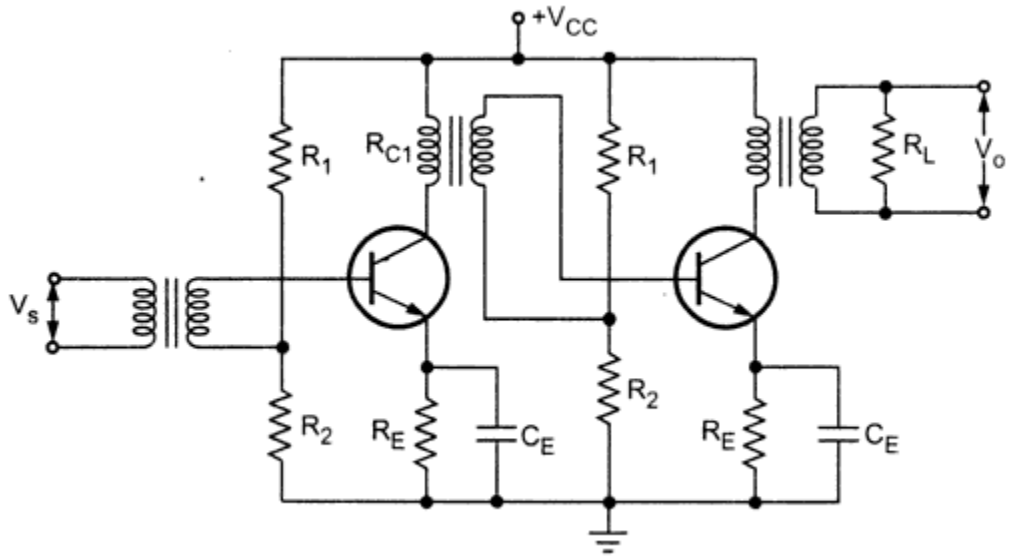
In multistage amplifier, the output signal of preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling, different types of coupling elements can be employed. These are :

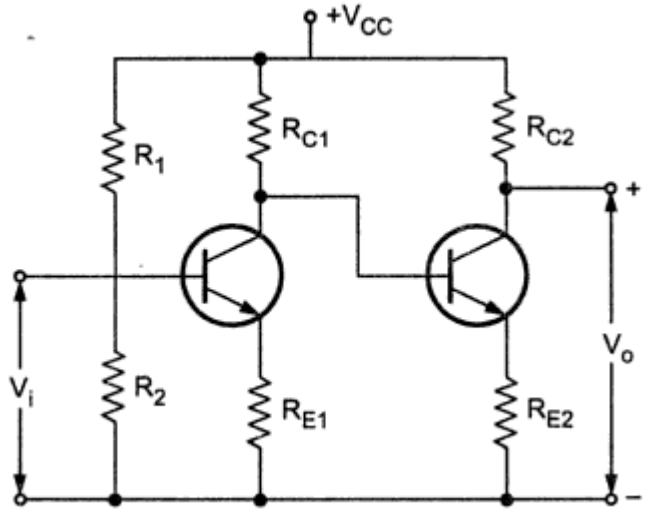
1. RC coupling
2. Transformer coupling
3. Direct coupling




**Two stage RC coupled amplifier using transistors**

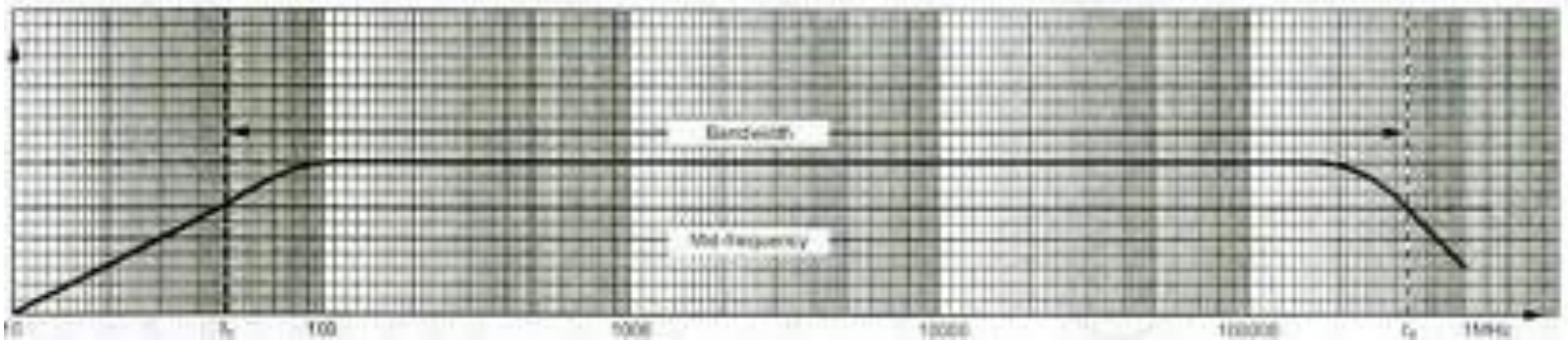
**Two stage transformer coupled amplifier using transistors**






**Two stage directly coupled amplifier using transistors**

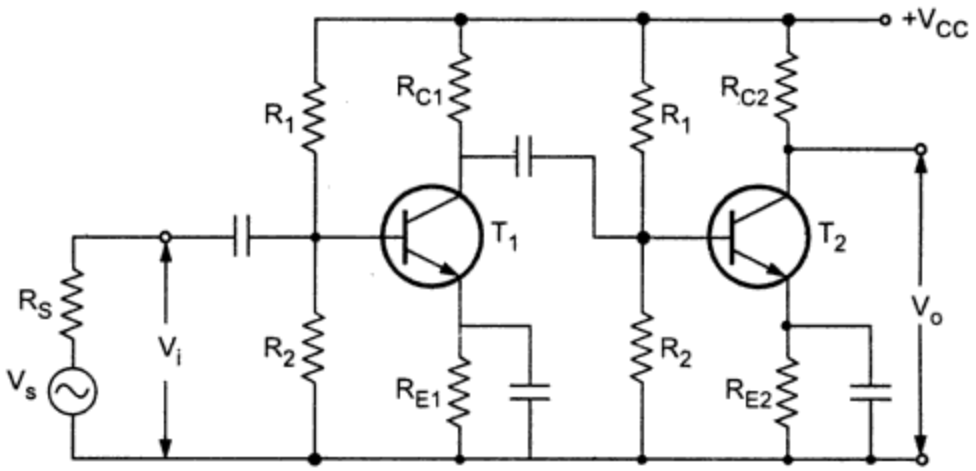
# Frequency Response of 2-Stage RC Coupled Amplifier



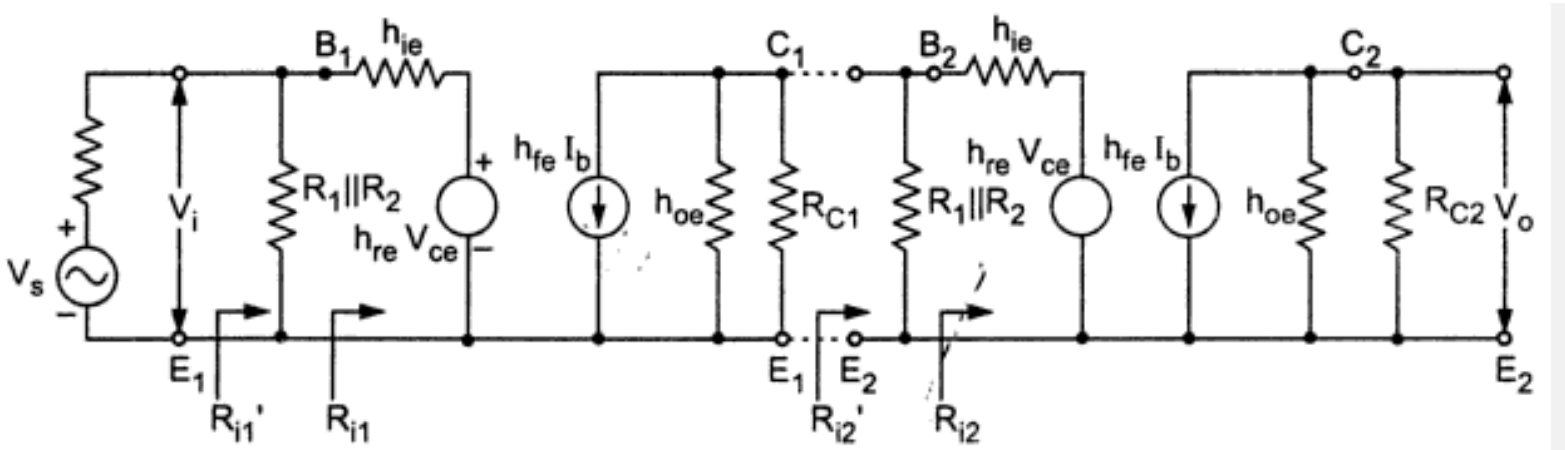
# Comparison Between Coupling Method

| Parameter | RC Coupled | Transformer Coupled | Direct Coupled |
|---|---|---|---|
| Coupling Components | Resistor and Capacitor | Impedance matching transformer | – |
| Block DC | Yes | Yes | No |
| Frequency response | Flat at middle frequencies | Not uniform, high at resonant frequency and low at other frequencies | Flat at middle frequencies and improvement in the low frequency response |
| Impedance matching | Not achieved | Achieved | Not achieved |
| DC amplification | No | No | Yes |
| Weight | Light | Bulky and heavy | |
| Drift | Not present | Not present | Present |
| Hum | Not present | Present | Not present |
| Application | Used in all audio small signal amplifiers. Used in record players, tape recorders, public address systems, radio receivers and television receivers. | Used in amplifier where impedance matching is an important criteria. Used in the output stage of the pubic address system to match the impedance of loudspeaker. Used in the RF amplifier stage of the receiver as a tuned voltage amplifier. | Used in amplification of slow varying parameters and where DC amplification is required. |

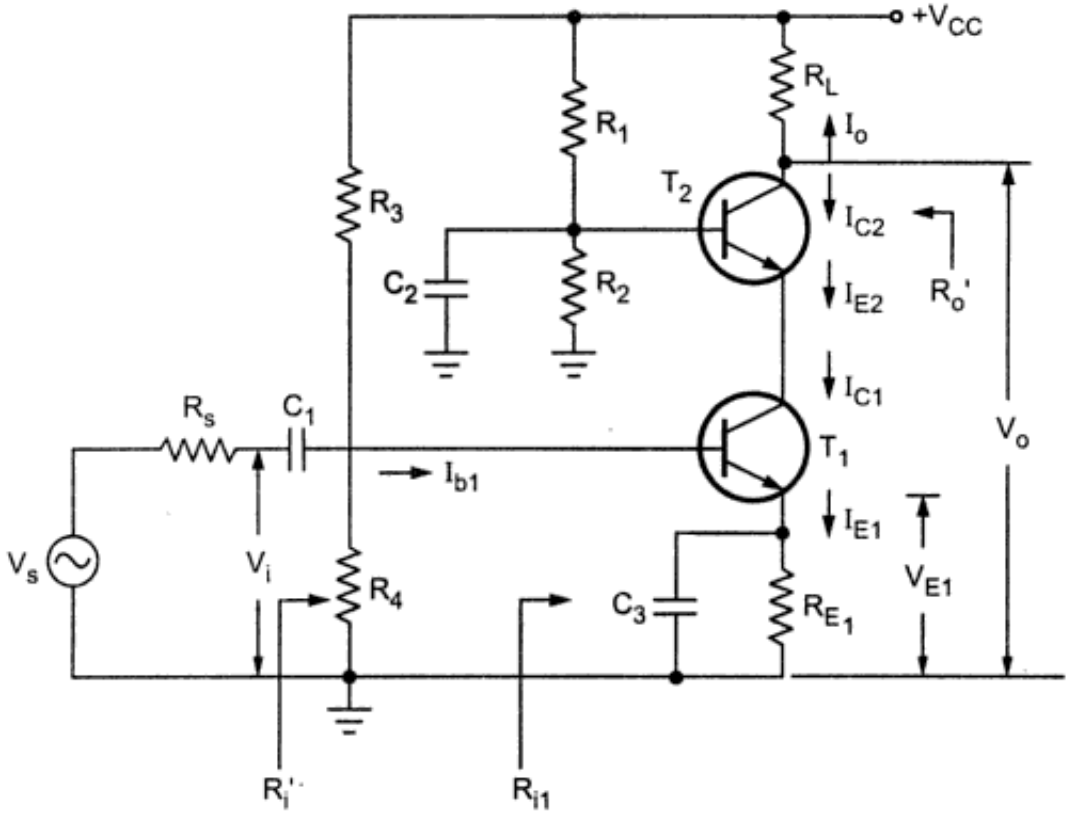
# CE-CE Cascade Amplifier



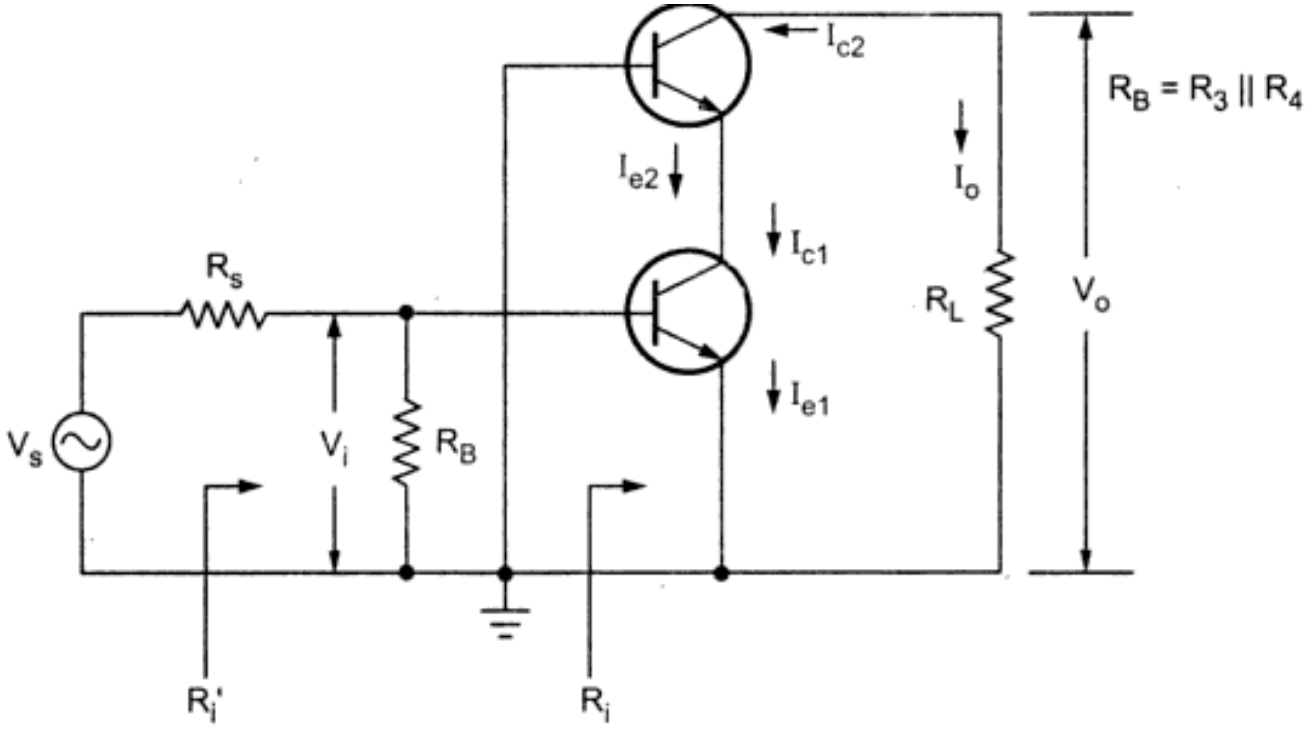
# h-parameter equivalent circuit for CE-CE cascade amplifier



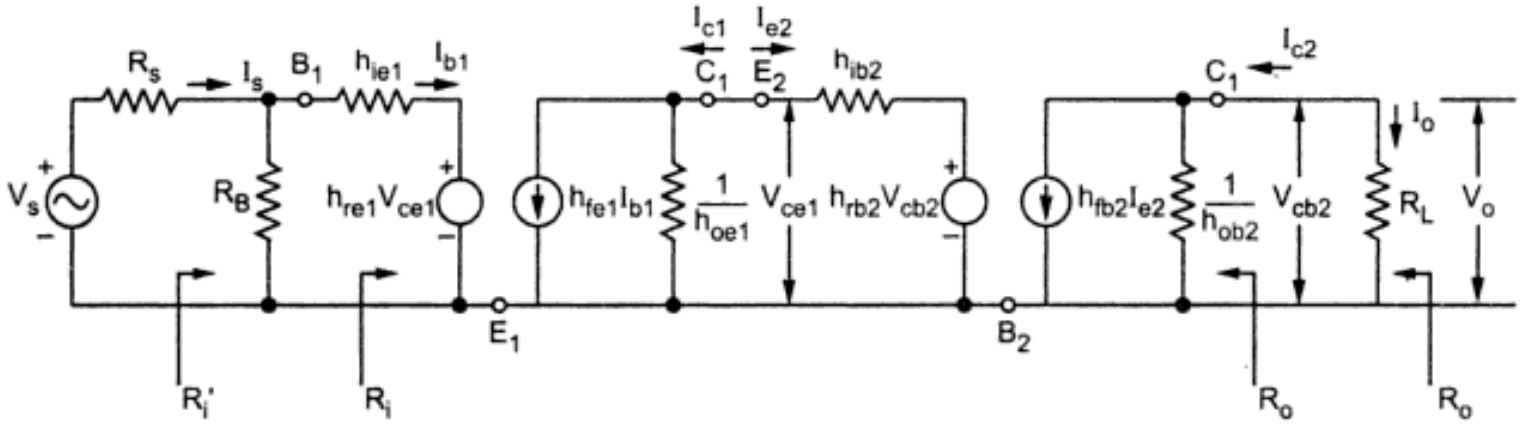
# Cascode Amplifier



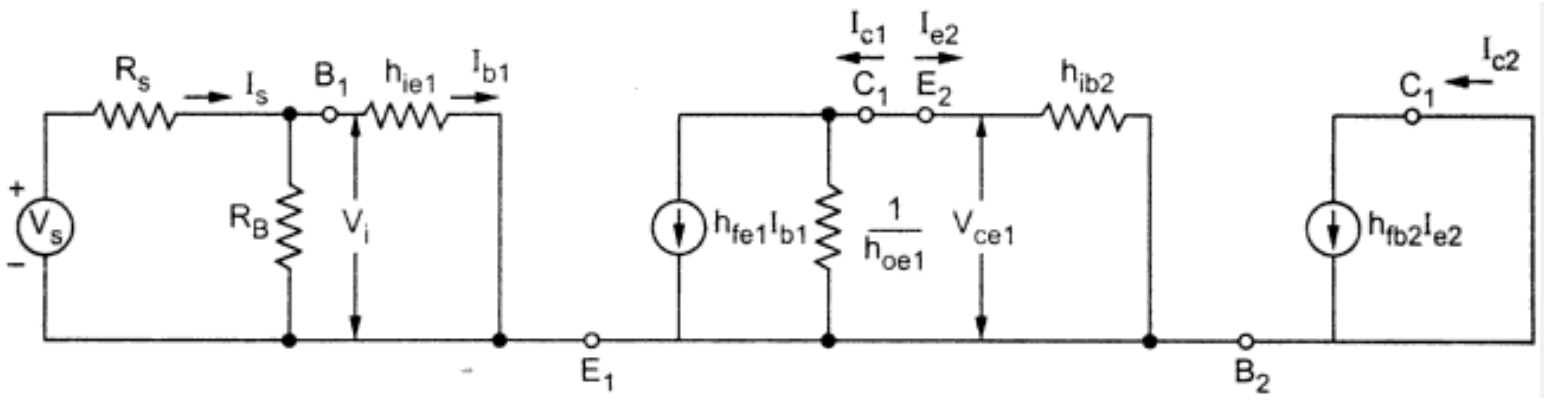
# AC equivalent circuit



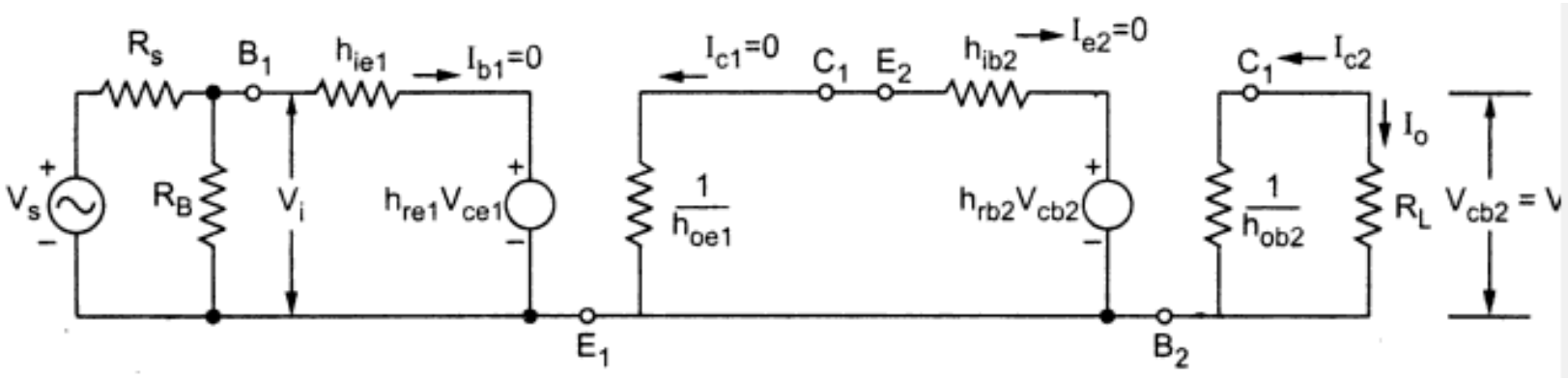
# h-parameter equivalent circuit for cascode amplifier



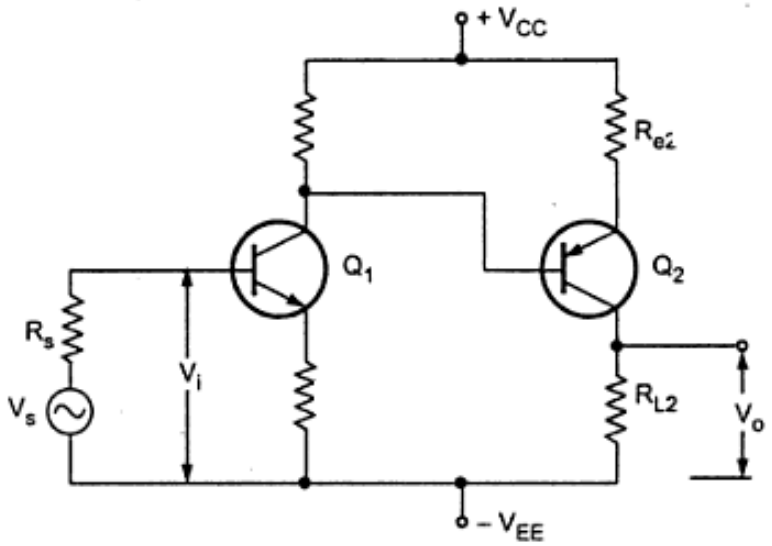
## h-parameter equivalent circuit when output shorted



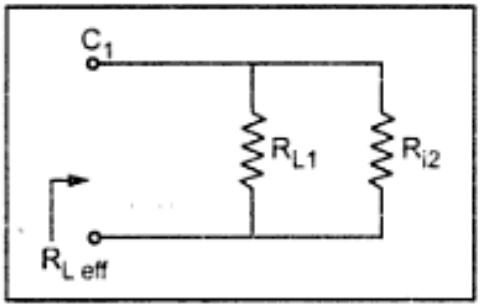
# h-parameter equivalent circuit when $I_b = 0$



# CE-CC Amplifier

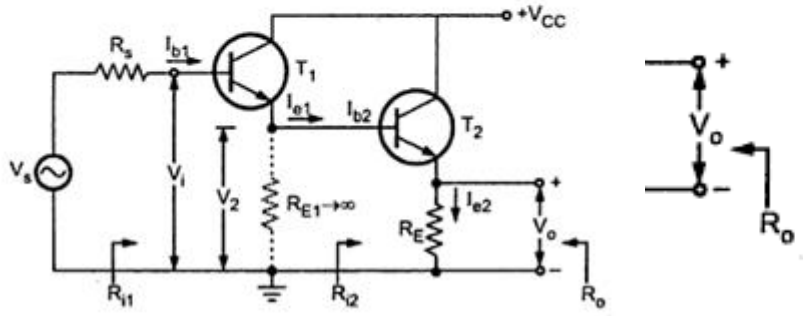



Analysis for first stage

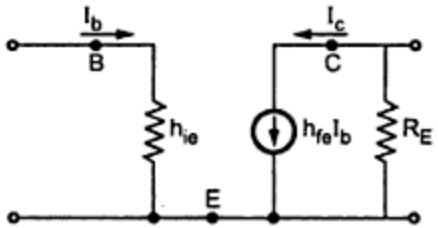


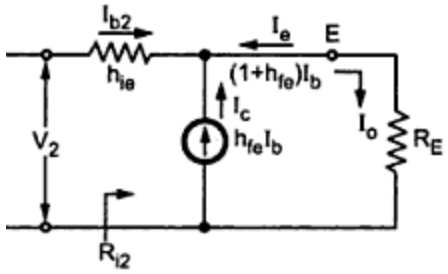
# Darlington Transistors

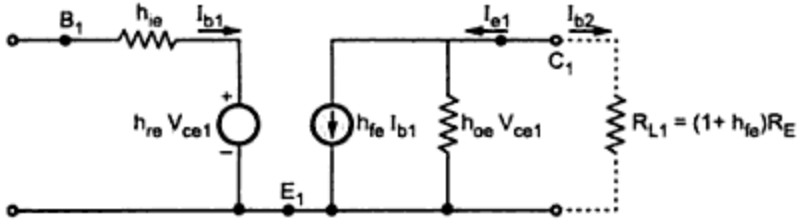
## Darlington Transistors

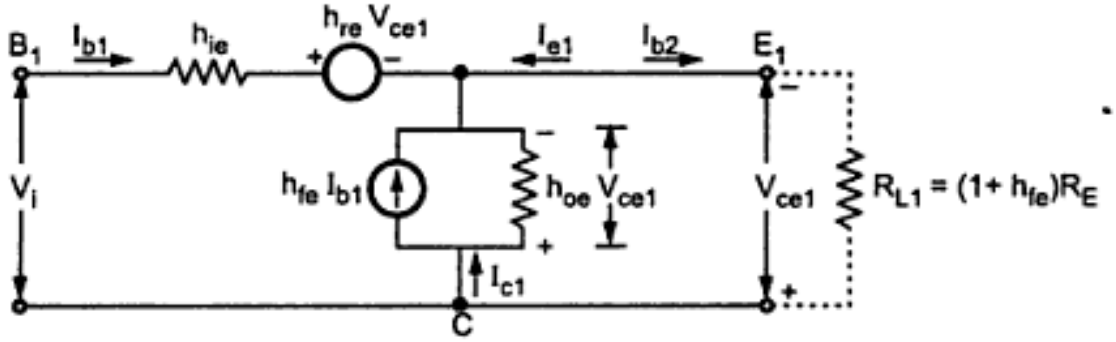


# AC Equivalent Circuit :



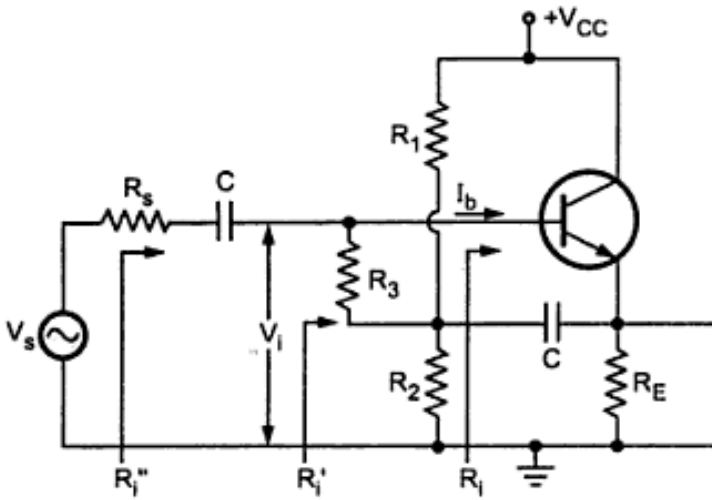



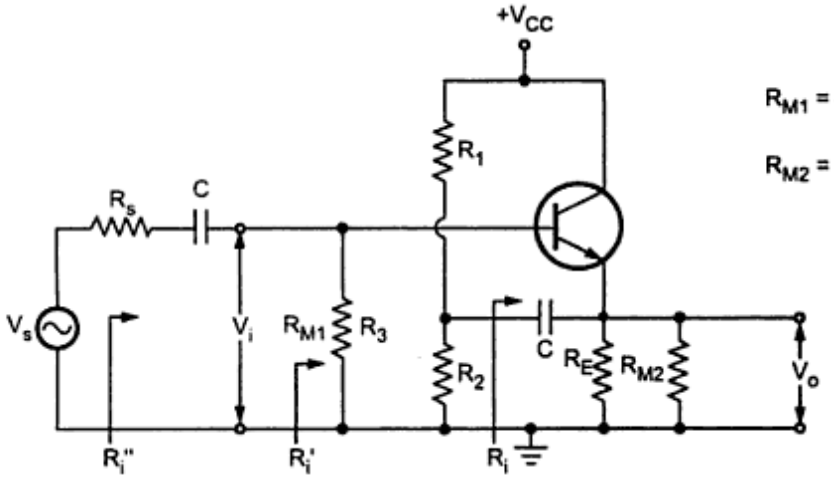






| Parameter | Single stage | Darlington |
|---|---|---|
| Input Resistance | $R_i = (1 + h_{fe})\, R_E = 168.3\ k\Omega$ | $R_i = \frac{(1+h_{fe})^2 R_E}{1+h_{oe}(1+h_{fe})R_E} \approx 1.65\ M\Omega$ |
| Current Gain | $A_i = 1 + h_{fe} = 51$ | $A_i = \frac{(1+h_{fe})^2}{1+h_{oe}(1+h_{fe})R_E} \approx 500$ |

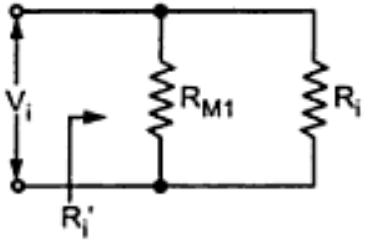
# Bootstrap Emitter Follower

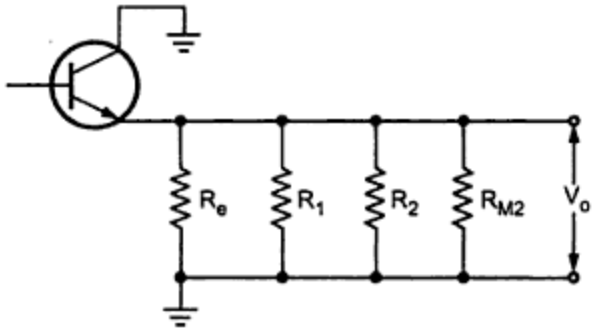


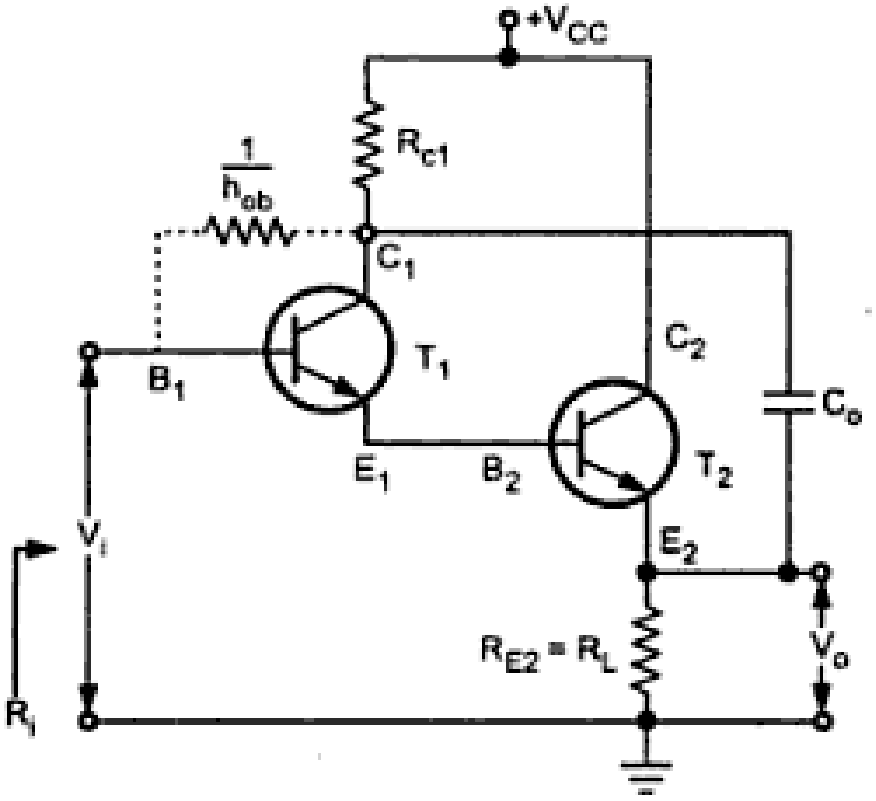

$$R_{M1} = \frac{R_3}{1 - A_v}$$

$$R_{M2} = \frac{R_3 A_v}{A_v - 1}$$

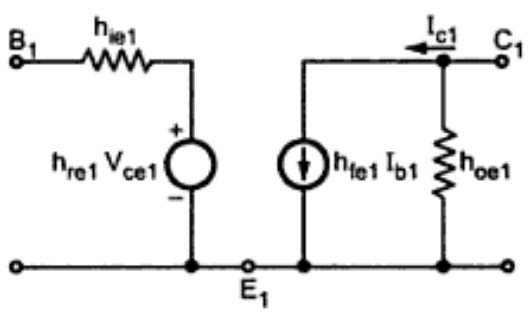



$R_e$
$R_1$
$R_2$
$R_{M2}$
$V_o$

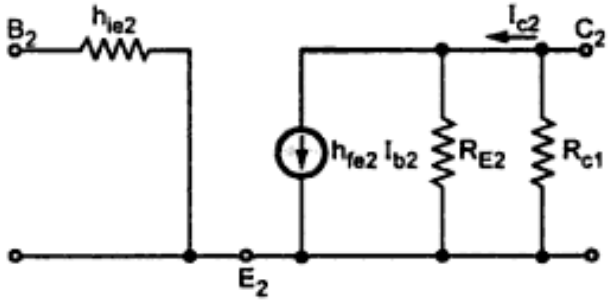
# Bootstrapped Darlington circuit



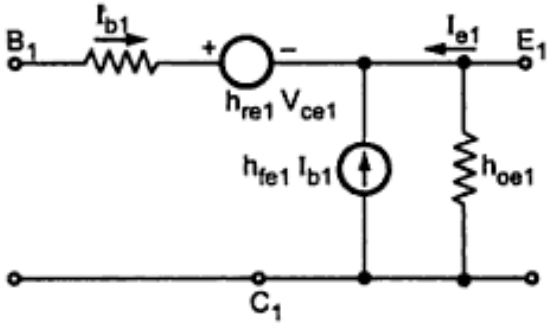
# AC Equivalent circuit for bootstrapped Darlington circuit



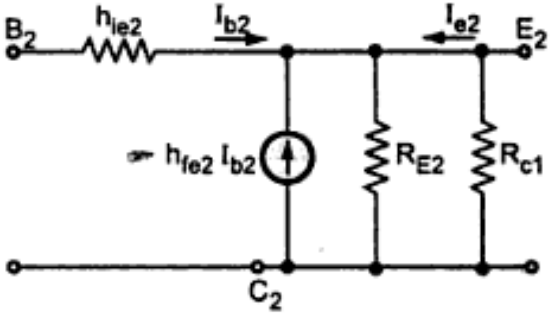

(a)



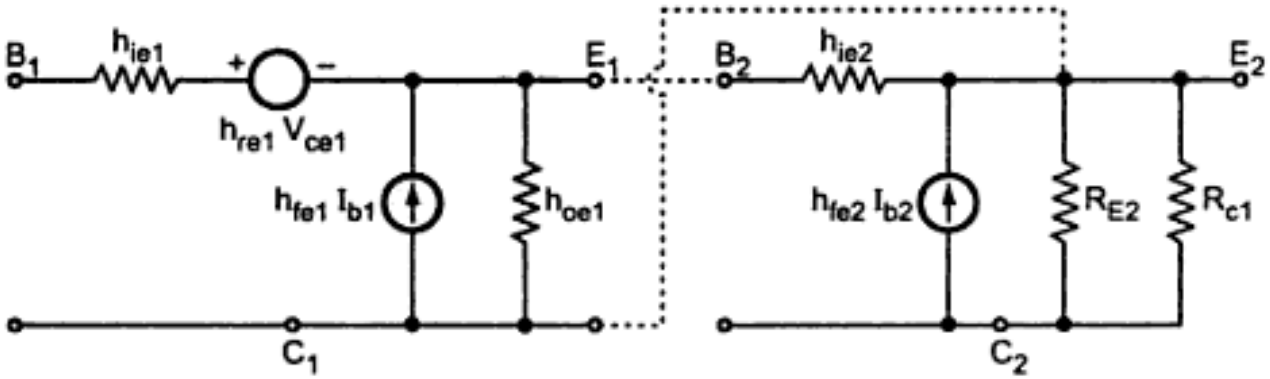

(b)

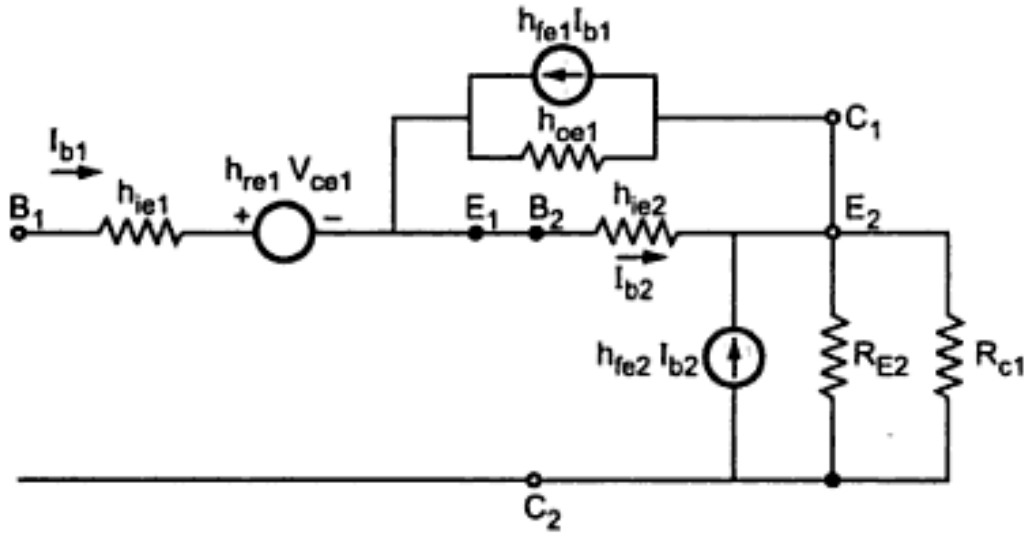



(c)

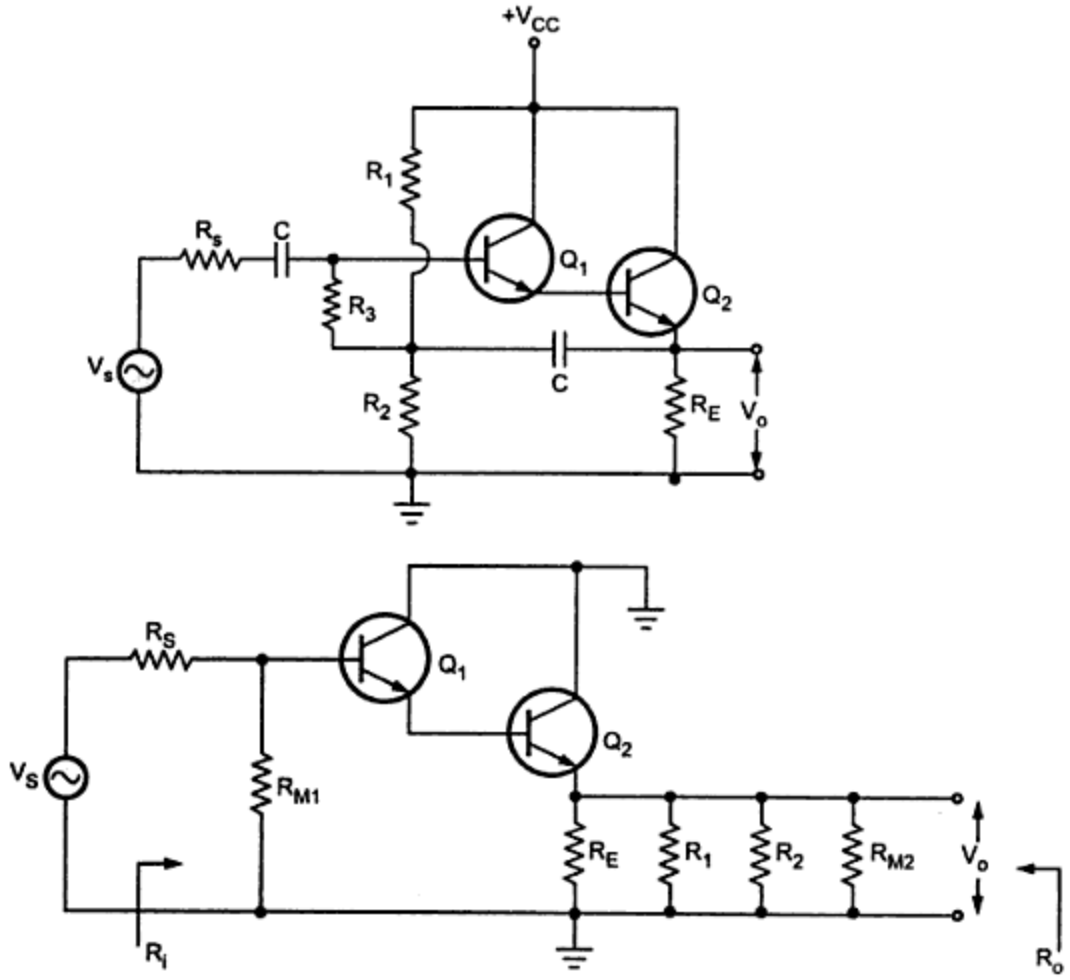



(d)


B1
hie1
+
−
hre1 Vce1
E1
B2
hie2
E2
hfe1 Ib1
hoe1
hfe2 Ib2
RE2
Rc1
C1
C2

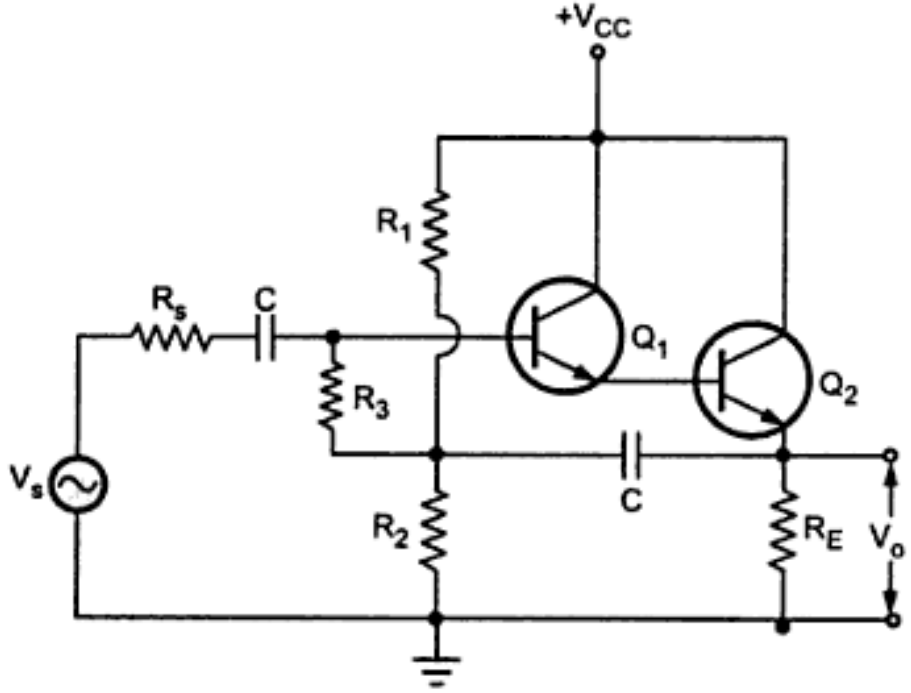

hfe1Ib1
hoe1
C1
Ib1
hre1 Vce1
hie1
B1
+
−
E1
B2
hie2
E2
Ib2
hfe2 Ib2
RE2
Rc1
C2

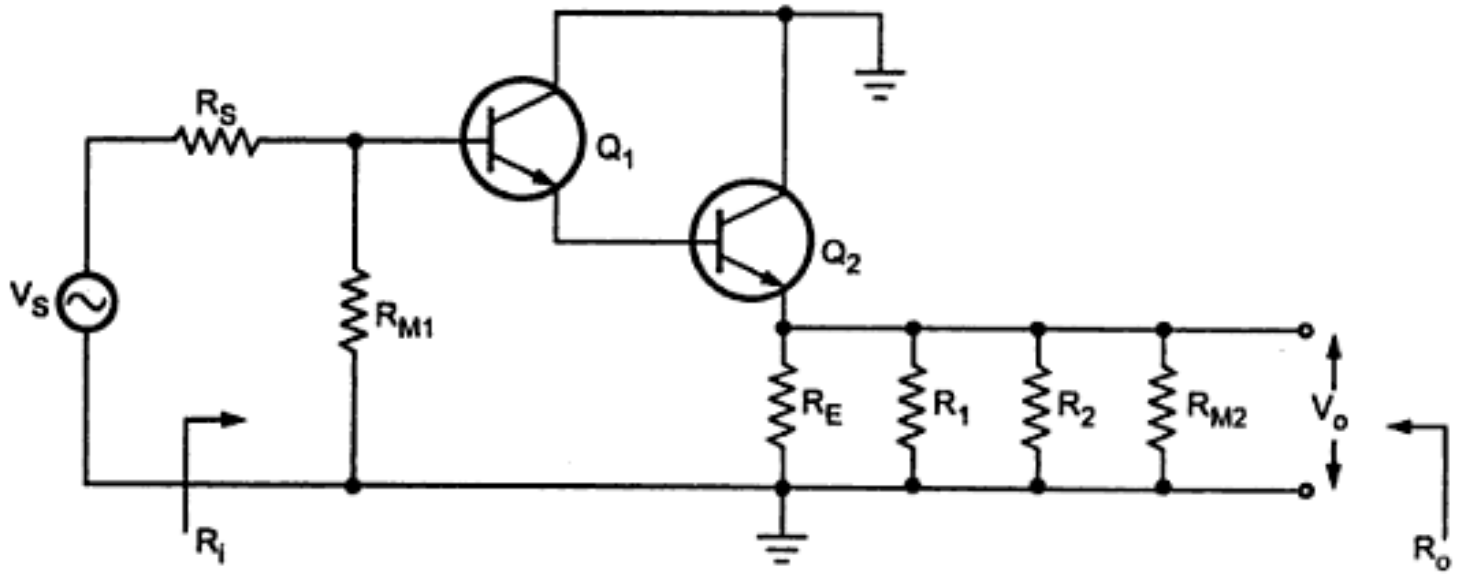
## Bootstrapped Darlington Circuit Alternative Approach




AC equivalent circuit

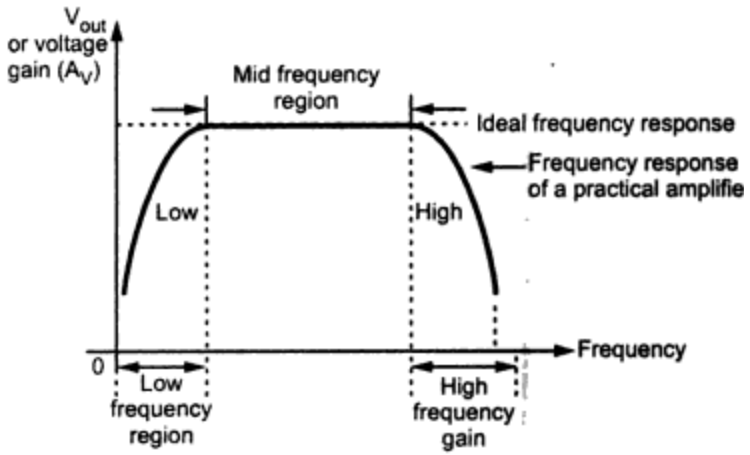
**Bootstrapped Darlington Circuit Alternative Approach**



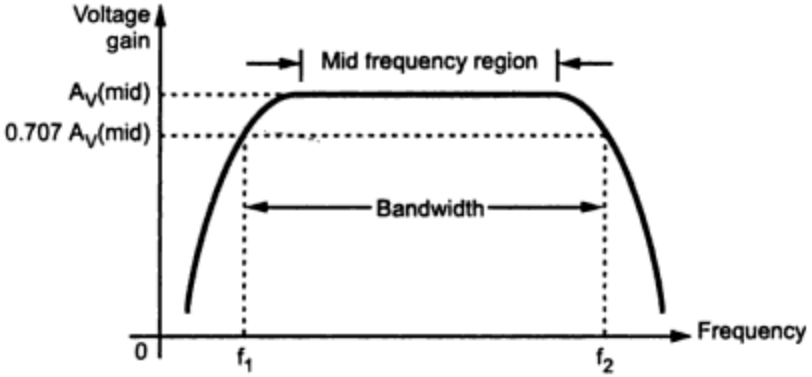



**AC equivalent circuit**

## Frequency Response of an RC Coupled Amplifier

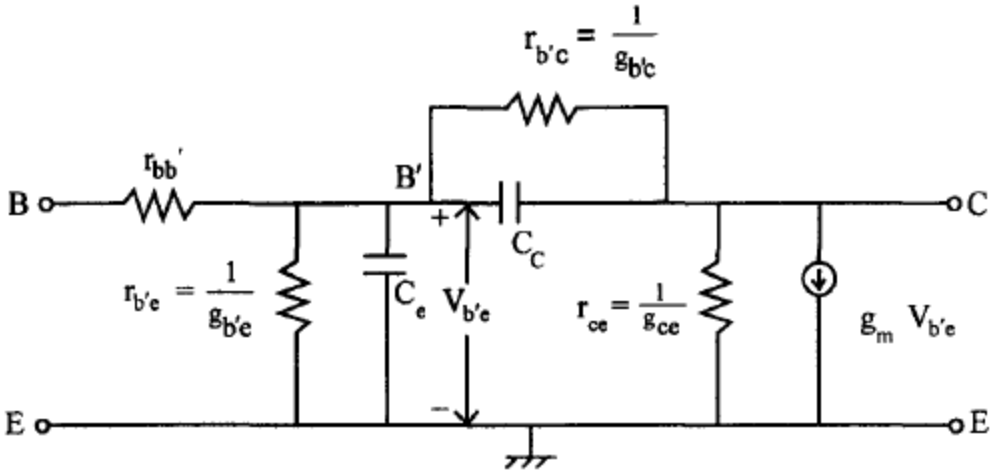



## Bandwidth of an Amplifier




**Frequency response, half power frequencies and bandwidth of an RC coupled amplifier**

# Hybrid – π Common Emitter Transc onductance Model




Hybrid - π C.E BJT Model

# UNIT-III

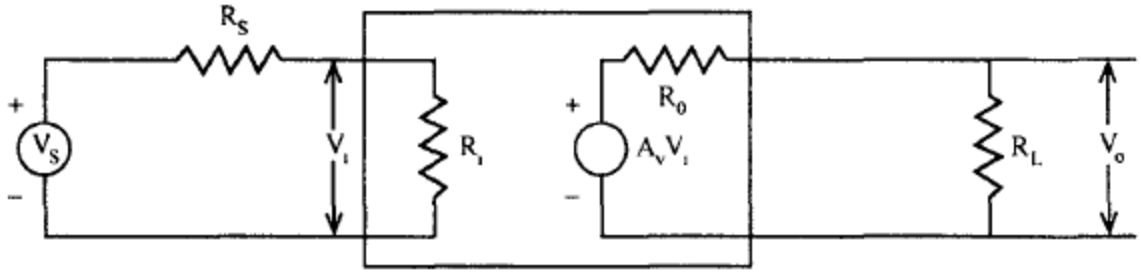
# Feedback Amplifiers & Oscillators

# CLASSIFICATION OF AMPLIFIERS

- Amplifiers can be classified broadly as,
- I. Voltage amplifiers.
- 2. Current amplifiers.
- 3. Transconductance amplifiers.
- 4. Transresistance amplifiers.

VOLTAGE AMPLIFIER

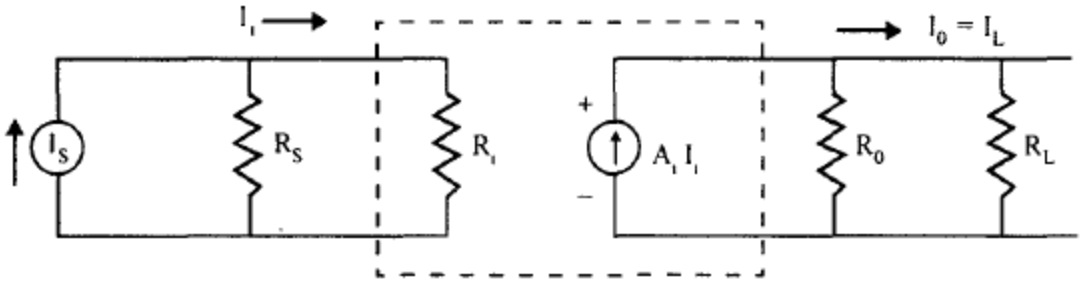
This circuit is a 2-port network and it represents an amplifier (see in Fig 7.1). Suppose Ri» Rs, drop across Rs is very small.




*Equivalent circuit of voltage amplifiers.*

CURRENT AMPLIFIER

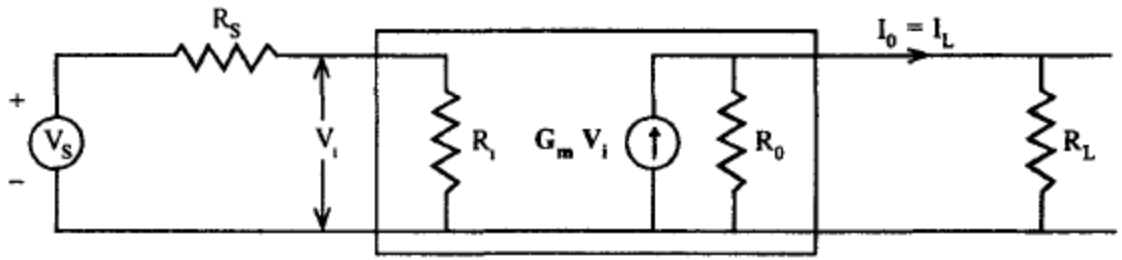
- An ideal current amplifier is one which gives output current proportional to input current and
- the proportionality factor is independent ofRs and RL.



TRANSCONDUCTANCE AMPLIFIER

Ideal Transconductance amplifier supplies output current which is proportional to input voltage

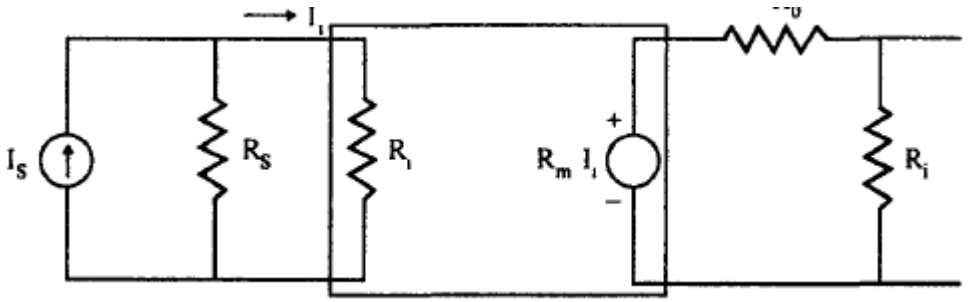
independently of the magnitude of Rs and RL.



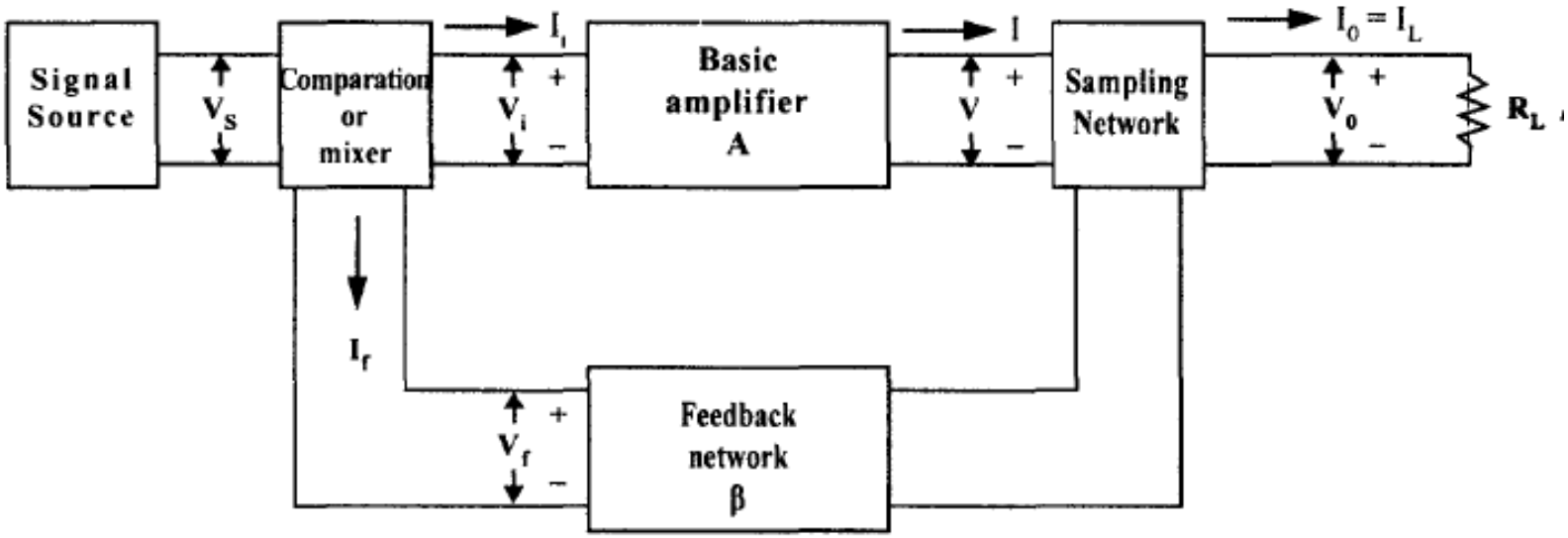
TRANS RESISTANCE AMPLIFIER

It gives output voltage Vo proportional to Is, independent of Rs a. RL. For *ideal amplifiers*

Rj =0, Ro=O



# GENERALIZED BLOCK SCHEMATIC



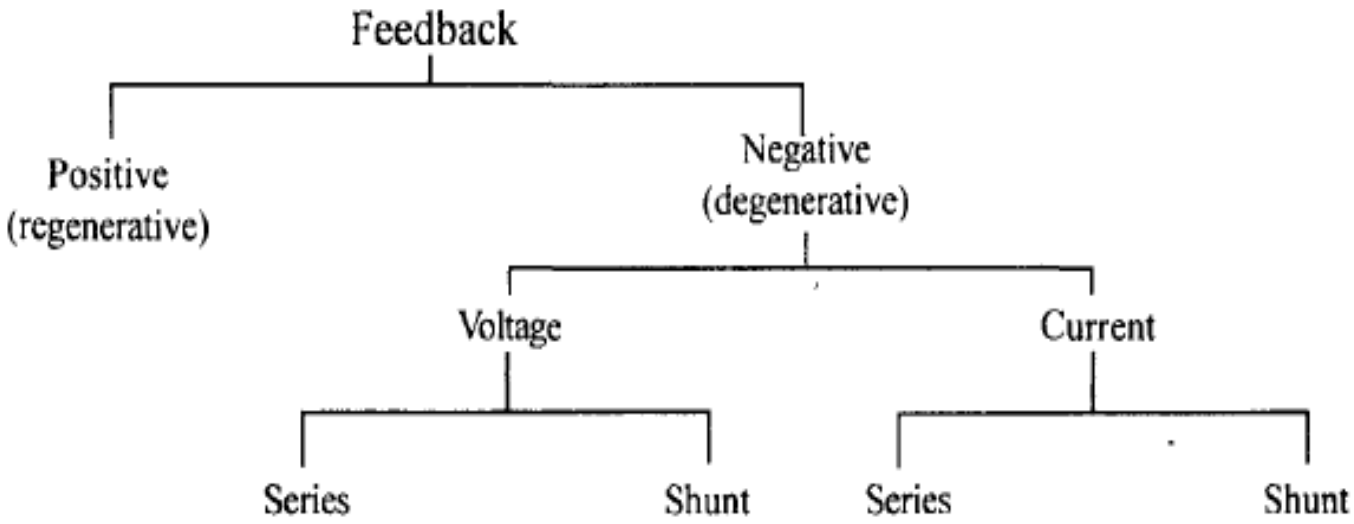
# Introduction To Feedback

- The process of injecting a fraction of output energy of some device back to the input is known as **feedback.**
- some of the short comings(drawbacks) of the amplifier circuit are:

1. Change in the value of the gain due to variation in supplying voltage, temperature or due to components.
2. Distortion in wave-form due to non linearities in the operating characters of the amplifying device.
3. The amplifier may introduce noise (undesired signals)

- The above drawbacks can be minimizing if we introduce feedback

# basic types of feedback in amplifiers



# Positive feedback

•When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called *positive feedback.*

•*Both amplifier* and feedback network introduce a phase shift of 180 . The result is a 360 phase shift around the loop, causing the *feedback voltage Vf to be in phase with the input signal Vin.*

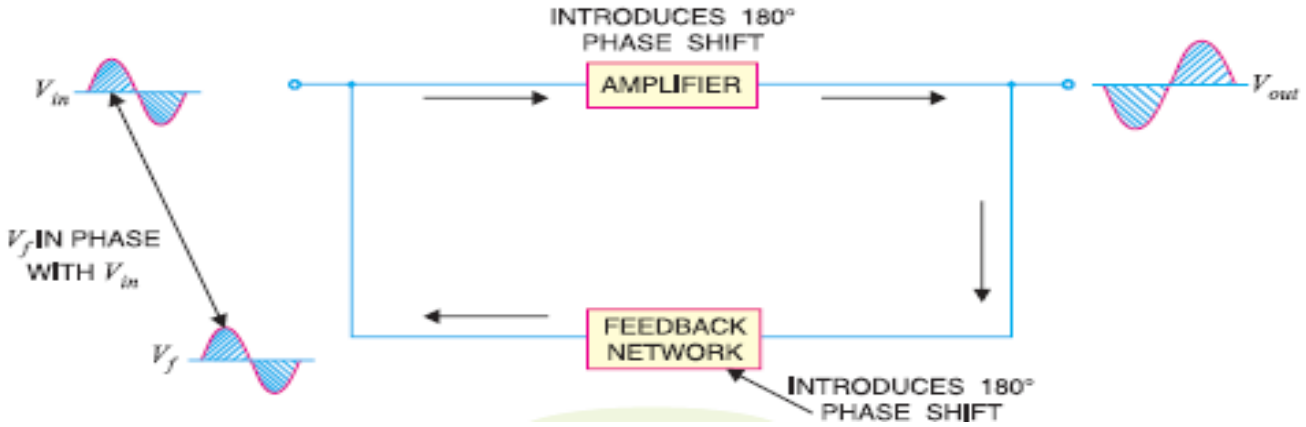



Fig. Block diagram for positive feedback

# Negative feedback.

•When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called *negative feedback.*
•The amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (*i.e., 0° phase shift).*
•Negative feedback is also called as *degenerative feedback.*

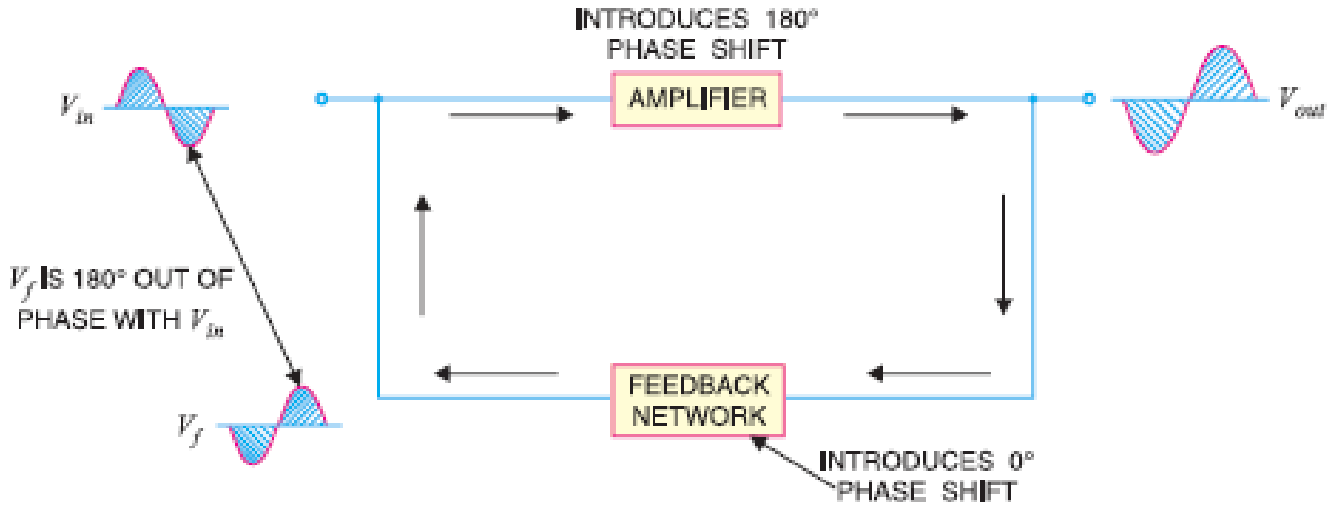
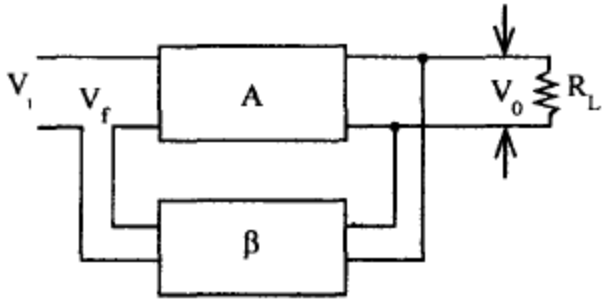
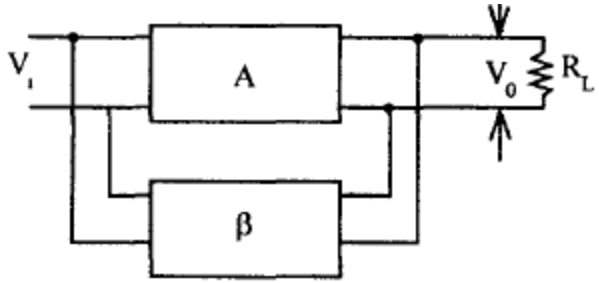



Fig.negative feedback amplifier

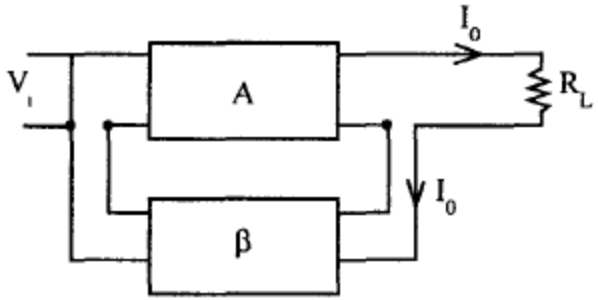
# CLASSIFACTION OF FEEDBACK AMPLIFIERS



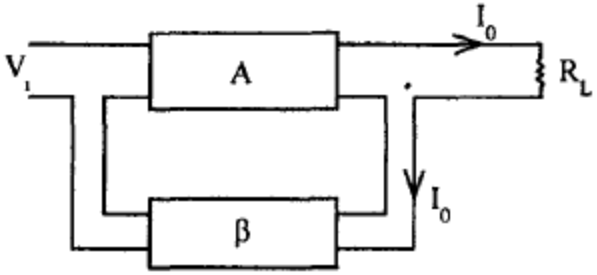

voltage series feedback.




Voltage shunt Feedback




Current Shunt Feedback




Current Series Feedback

$$A_{Vf} = \frac{V_o}{V_s}$$

$$A_{If} = \frac{I_o}{I_s}$$

$$G_{Mf} = \frac{I_o}{V_s}$$

$$R_{Mf} = \frac{V_o}{I_s}$$

EFFECT OF NEGATIVE FEEDBACK ON TRANSFER GAIN

- REDUCTION IN GAIN

$$A'_V = \frac{A_v}{1 + \beta A_v} \qquad \text{Denominator is} > 1. \quad \therefore \quad A'_V < A_V$$

- INCREASE IN BANDWIDTH

$$f_H' = f_H (1 + \beta_v A_{v\,(mid)})$$

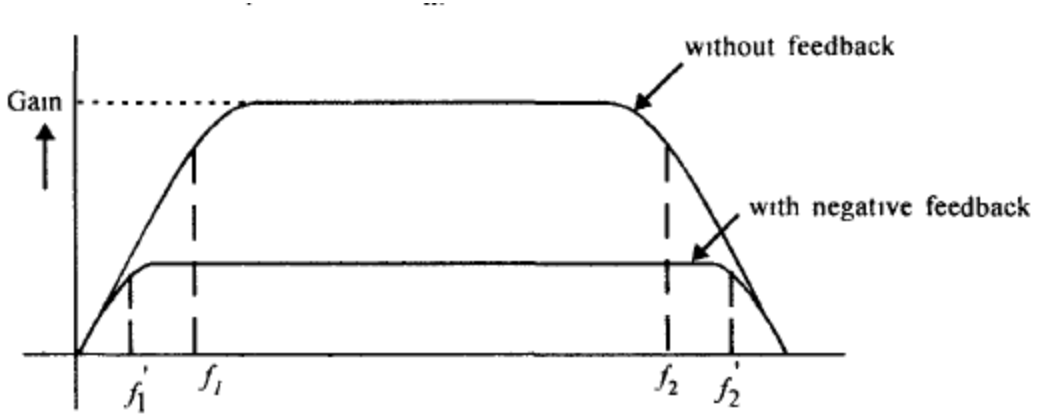
$$f_L' = \frac{f_L}{1 + \beta_v A_{v(mid)}}$$

- REDUCTION IN DISTORTION

$$\frac{D}{1 + \beta_v A_v} \text{ is } < D$$

- FEEDBACK TO IMPROVE SENSITIVITY
- FREQUENCY DISTORTION
- BAND WIDTH

$$(BW)_f = (1 + \beta A_m)\, BW$$



❖ SENSITIVITY OF TRANSISTOR GAIN

$$\textit{Sensitivity} = \frac{\left|\frac{dA_f}{A_f}\right|}{\left|\frac{dA}{A}\right|}$$

$$\textit{Densitivity} \quad \boxed{D = (1 + \beta A).}$$

❖ REDUCTION OF NONLINEAR DISTORTION

$$B_{2f} = \frac{B_2}{1 + \beta A} \quad B_{2f} < B_2$$

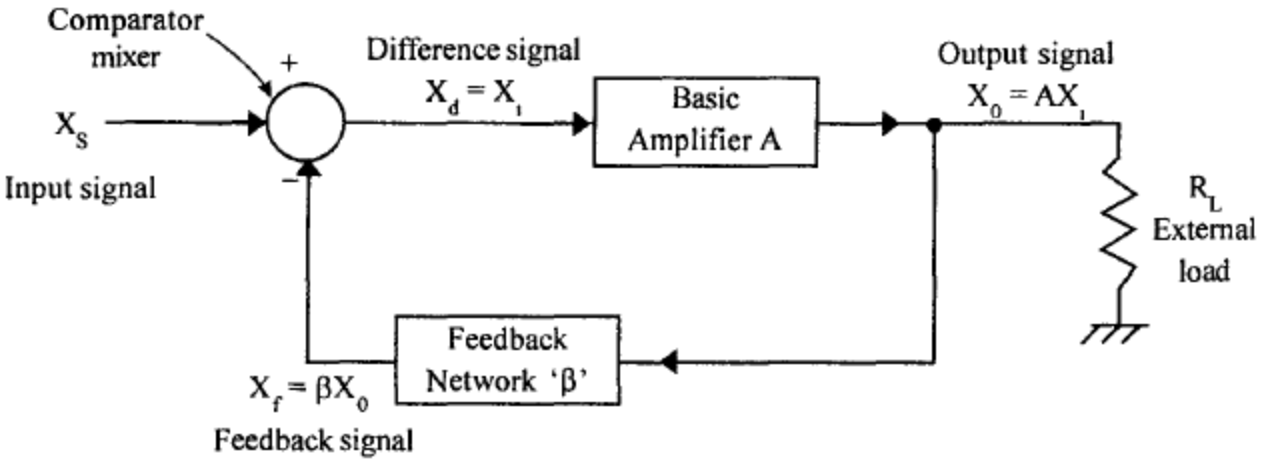
❖ REDUCTION OF NOISE

$$N_F = \frac{N}{1+\beta A}$$

$N_F < N$. Noise is reduced with negative feedback.

TRANSFER GAIN WITH FEEDBACK

Consider the generalized feedback amplifier



$$A_f = \frac{A}{1+\beta A}$$

$A_f$ = gain with feedback.

A = transfer gain without feedback.

If $|A_f| < |A|$ the feedback is called as negative or degenerative, feedback

If $|A_f| > |A|$ the feedback is called as positive or regenerative, feedback

LOOP GAIN

***Return Ratio***

βA = Product of feedback factor β and amplification factor A is called as *Return Ratio.*

***Return Difference (D)***

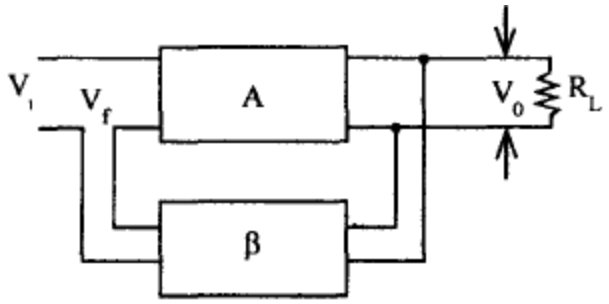
The difference between unity (1) and return ratio is called as *Return difference.*

$$D = 1 - (-\beta A) = 1 + \beta A.$$

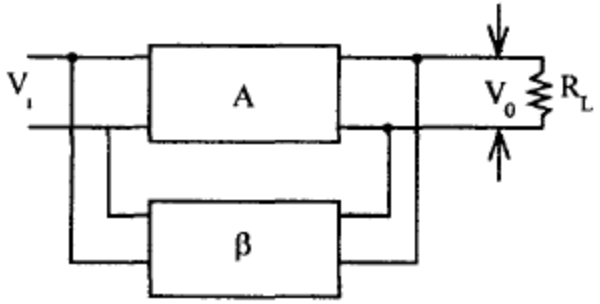
# CLASSIFACTION OF FEEDBACK AMPLIFIERS

**There are four types of feedback,**

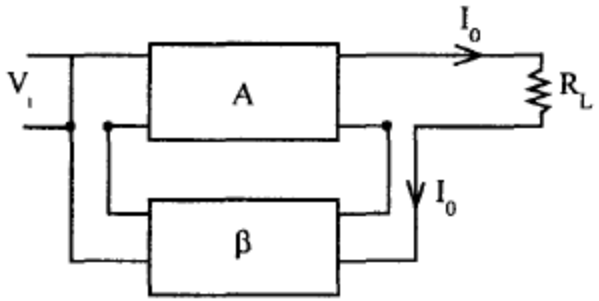
1. Voltage series feedback.
2. Voltage shunt feedback.
3. Current shunt feedback.
4. Current series feedback



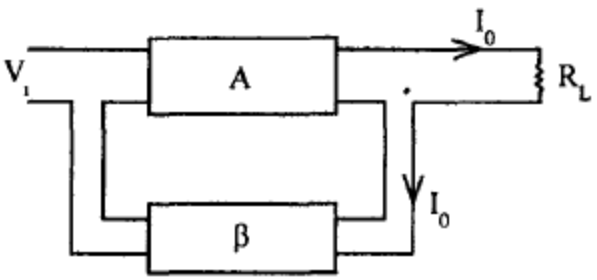

*voltage series feedback.*




*Voltage shunt Feedback*




*Current Shunt Feedback*




*Current Series Feedback*

**EFFECT OF FEEDBACK ON INPUT RESISTANCE**

*Voltage shunt Feedback*

$$R_i' = \frac{R_i}{(1+\beta_i A_i)}$$

*Current Shunt Feedback*

$$R_{if} = \frac{V_i}{(1+\beta A_I)I_i} = \frac{R_i}{1+\beta.A_I}$$

*voltage series feedback.*

$$R_{if} = R_i (1+\beta A)$$

*Current Series Feedback*

$$R_{If} = R_I\left(1+\beta.\frac{V_0}{V_I}\right) = R_I(1+\beta.A_V)$$

EFFECT OF NEGATIVE FEEDBACK ON Ro

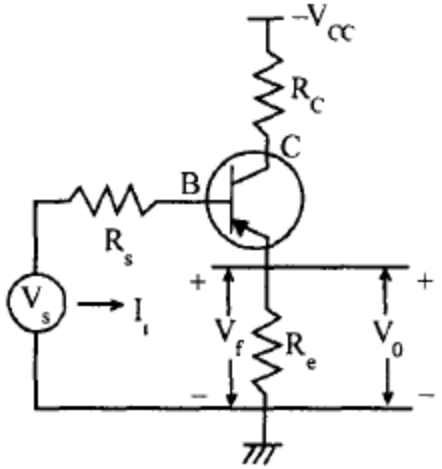
*voltage series feedback.*

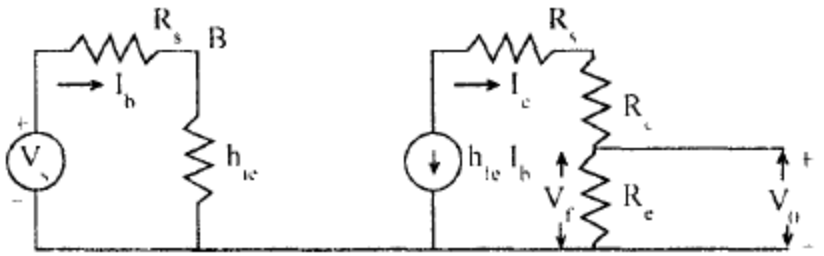
$$R_{of}' = \frac{\frac{R_o}{1+\beta A_V} \times R_L}{\frac{R_0}{1+\beta A_V} + R_L} = \frac{R_o R_L}{R_o + R_L + \beta.A_v R_L}$$

*Current Shunt Feedback*

$$\boxed{R_{of}' = R_0 (1+ \beta A_i)}$$

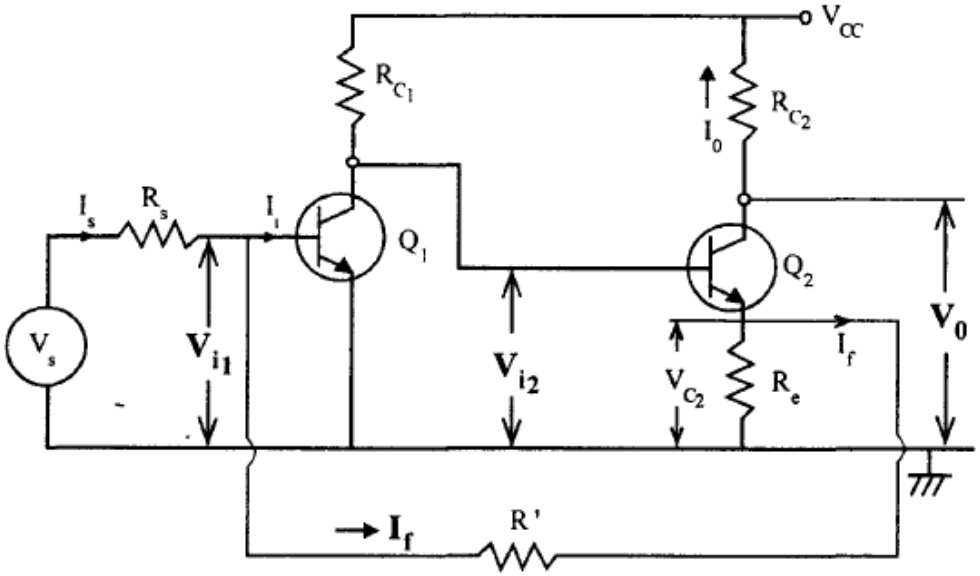
## ANALYSIS OF FEEDBACK AMPLIFIERS

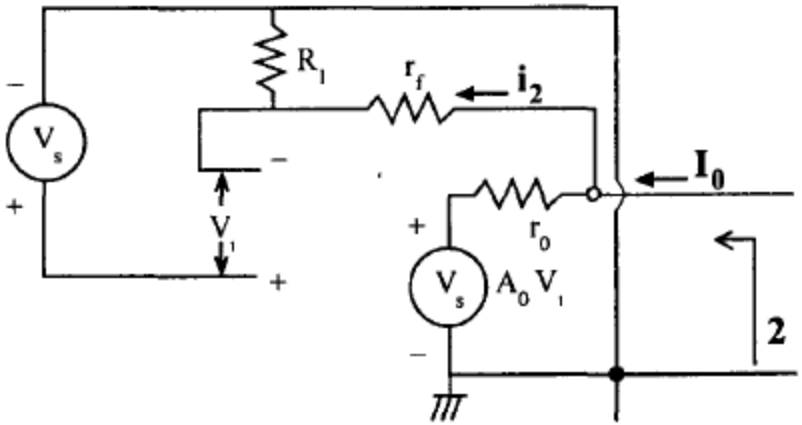



***Block Schematic***

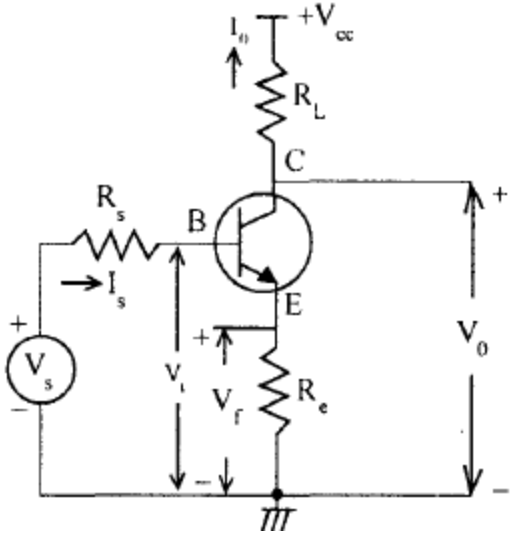
***Current shunt feedback.***



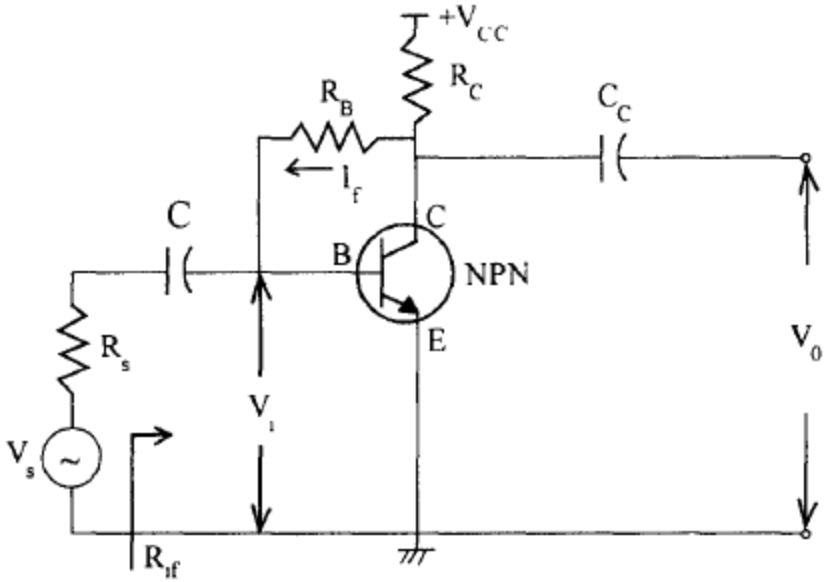




***Equivalent circuit.***

CURRENT SERIES FEEDBACK

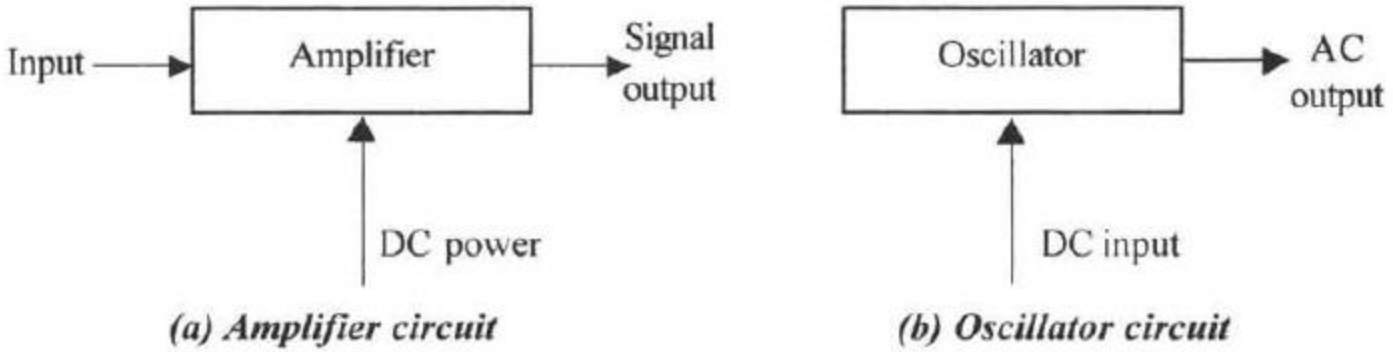



VOLTAGE SHUNT FEEDBACK



# OSCILLATORS

Oscillator is a source of AC voltage or current.



# Oscillator Circuit

- Oscillator is an electronic circuit which converts dc signal into ac signal.
- Oscillator is basically a positive feedback amplifier with unity loop gain.
- For an inverting amplifier- feedback network provides a phase shift of 180° while for non-inverting amplifier- feedback network provides a phase shift of 0° to get positive feedback .

$$\frac{V_o}{V_s} = \frac{A}{1 - A\beta}$$

If βA=1 then $V_o = \infty$ ; Very high output with zero input.

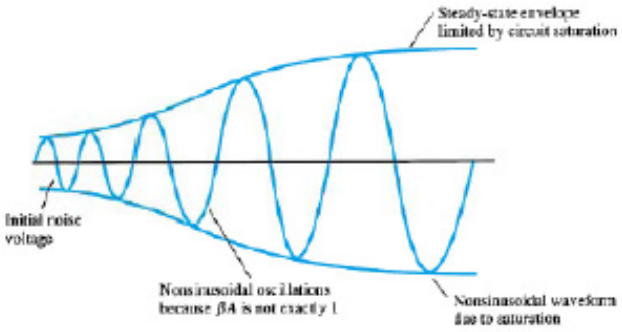
Use positive feedback through frequency-selective feedback network to ensure sustained oscillation at $\omega_0$

# Use of Oscillator Circuits

- Clock input for CPU, DSP chips …
- Local oscillator for radio receivers, mobile receivers, etc
- As a signal generators in the lab
- Clock input for analog-digital and digital-analog converters

# Oscillators

- If the feedback signal is not positive and gain is less than unity, oscillations dampen out.
- If the gain is higher than unity then oscillation saturates.




# Type of Oscillators

Oscillators can be categorized according to the types of feedback network used:

- RC Oscillators: Phase shift and Wien Bridge Oscillators
- LC Oscillators: Colpitt and Hartley Oscillators
- Crystal Oscillators

**There are two types of oscillators circuits:**

**I. Harmonic Oscillators** **2. Relaxation Oscillators**

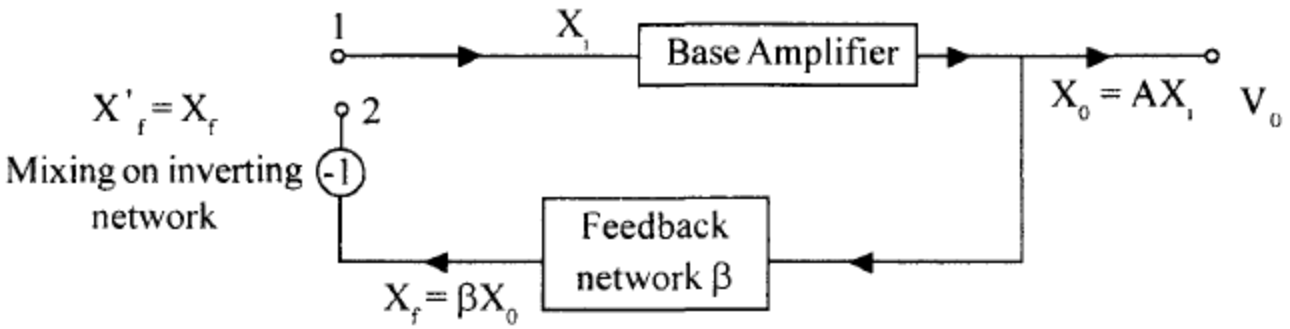
**PERFORMANCE MEASURES OF OSCILLATOR CIRCUITS:**

- ***Stability:***
- ***Amplitude stability:***
- ***Output Power:***
- ***Harmonics:***

Total phase shift = $360^0$ (180 + 180). Therefore, to get sustained oscillations,

1. The loop gain must be unit 1.
2. Total Loop phase shift must be $0^0$ or $360^0$. (Amplifier circuit produces $180^0$ phase shift and feedback network another $180^0$.

## SINUSOIDAL OSCILLATORS

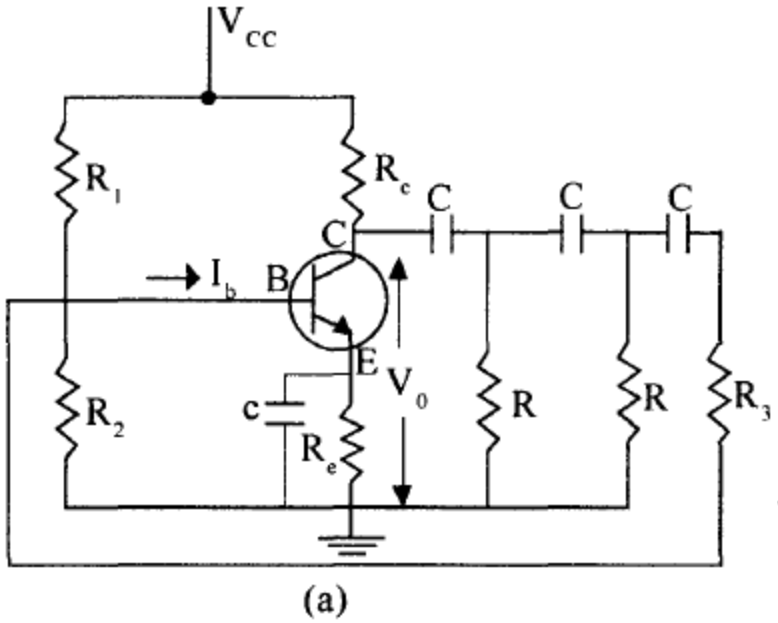



*Block schematic*

# BARKHAUSEN CRITERION

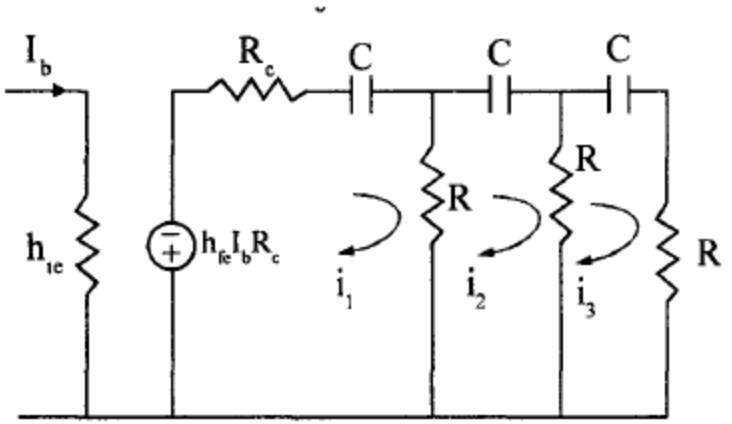
$$|\beta A| = 1 \text{ and phase of } -A\beta = 0.$$

# R - C PHASE-SHIFT OSCILLATOR




(a)

***Transistor phase shift oscillator.***




***R - C Equivalent circuit.***

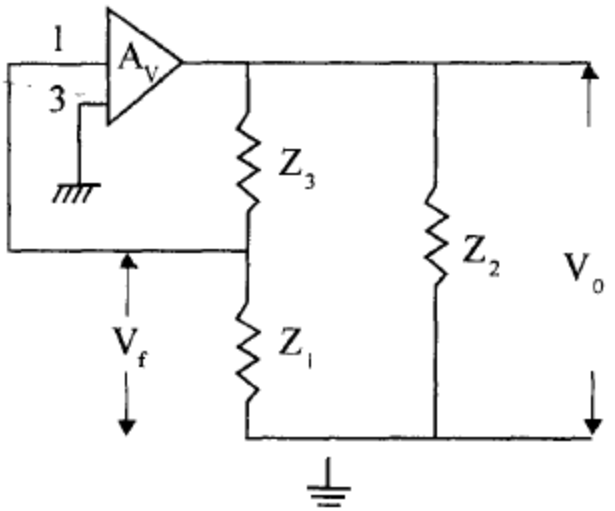
$$h_{fe} K > 4K^2 + 23K + 29$$

$$h_{fe} > 4K + 23 + \frac{29}{K}$$

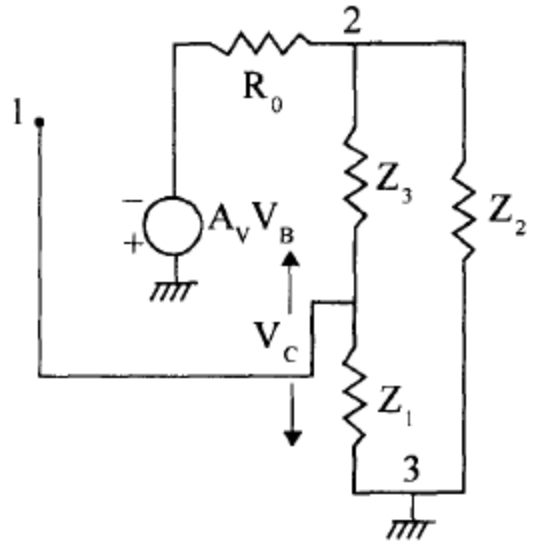
$$K < 2.7$$

$$h_{fe} > 44.5$$

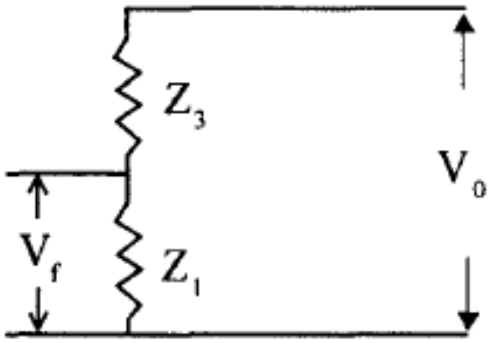
# A GENERAL FORM OF LC OSCILLATOR CIRCUIT




(a)




(b)

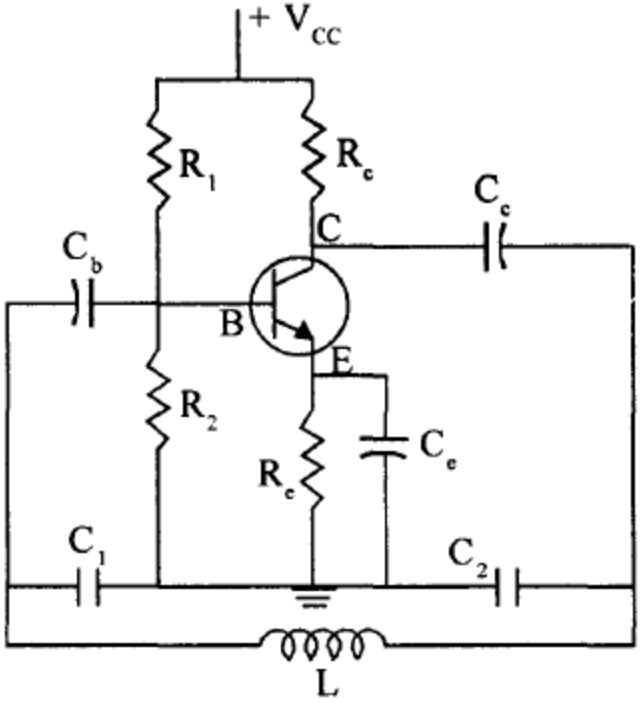



$$-A\beta = \frac{A_V X_1}{X_2}.$$

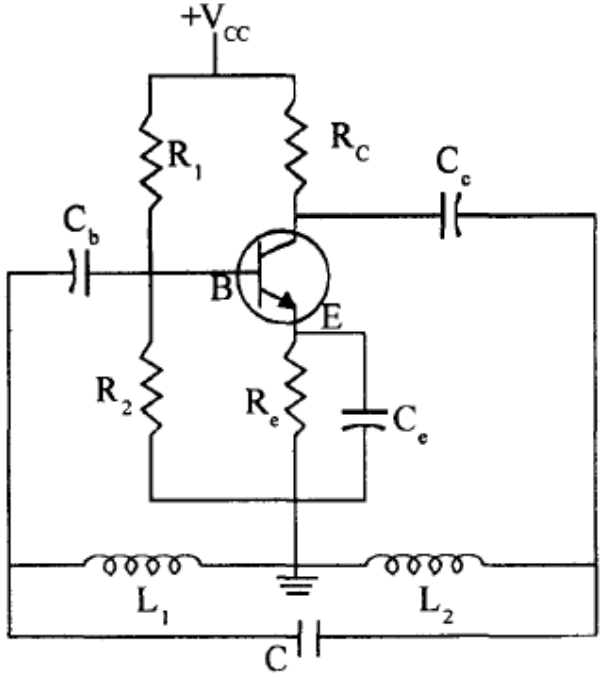
- Aβ must be positive, and at least unity in magnitude. Than XI and X2 must have the same sign.

So if $X_1$ and $X_2$ are capacitive, $X_3$ should be inductive and vice versa.

If $X_1$ and $X_2$ are capacitors, the circuit is called ***Colpitts Oscillator***
If $X_1$ and $X_2$ are inductors, the circuit is called ***Hartely Oscillators***




*(a) Colpitts oscillator*



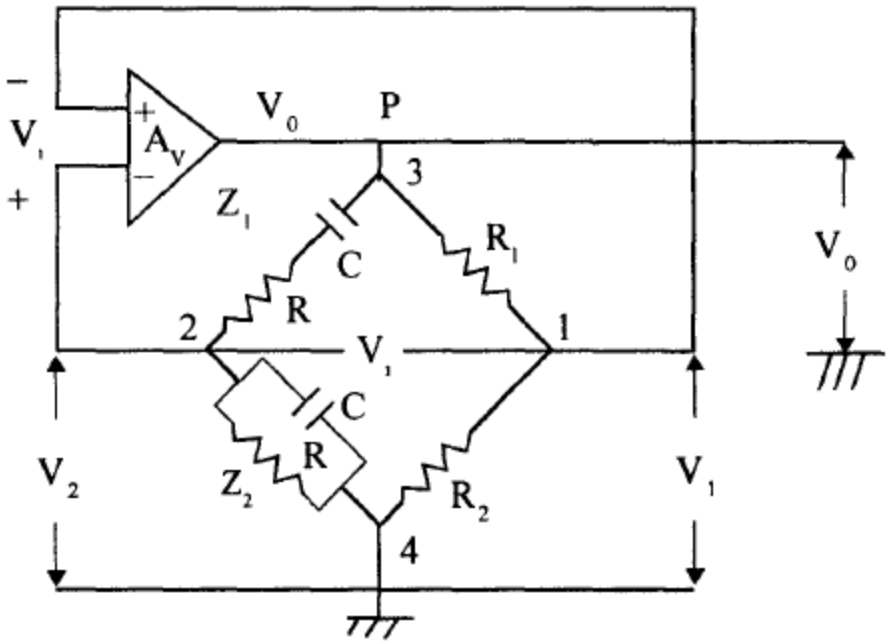

*(b) Hartely oscillator circuit*

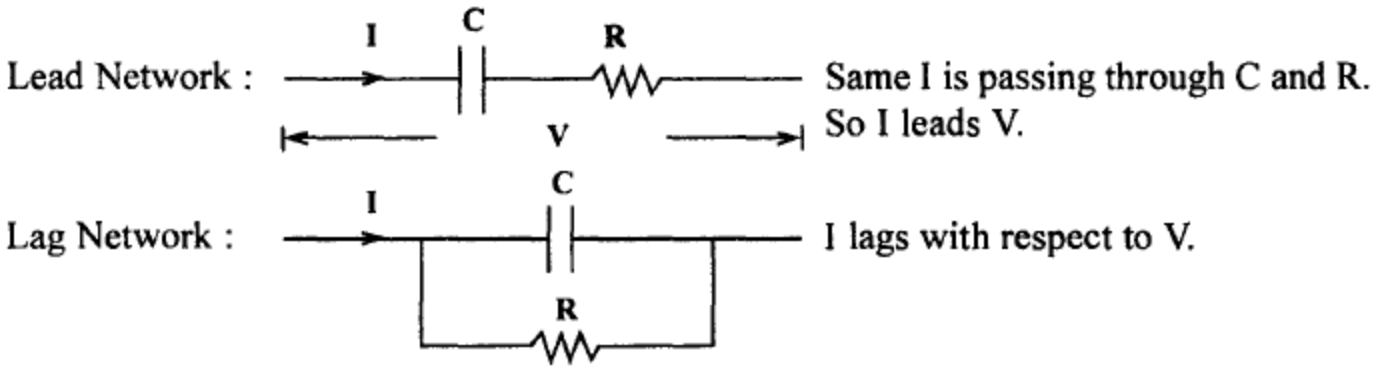
$$f = \frac{1}{2\pi\sqrt{L C_T}}$$

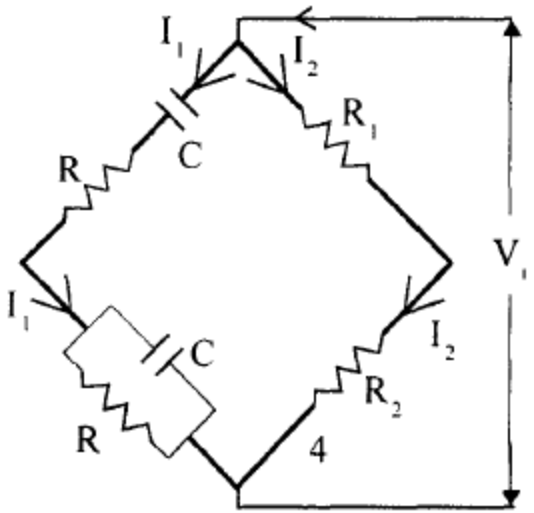
where $C_T = \frac{C_1 C_2}{C_1 + C_2}$

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2) C_3}}$$

***Wien bridge oscillator circuit.***



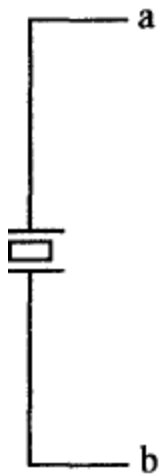



***Wien Bridge oscillator circuit.***

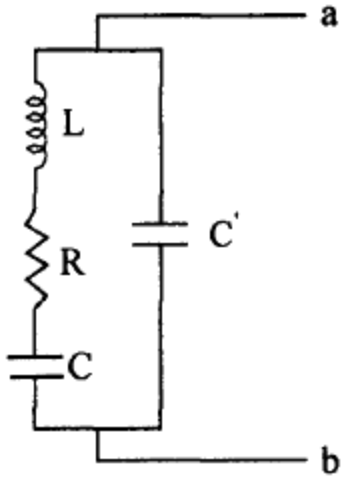
$$\boxed{f = \frac{1}{2\pi RC}}$$

$$\boxed{h_{fe} = 4k + 23 + \frac{29}{K}.}$$

# CRYSTAL OSCILLATORS




*Crystal*




*Electrical Model*

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

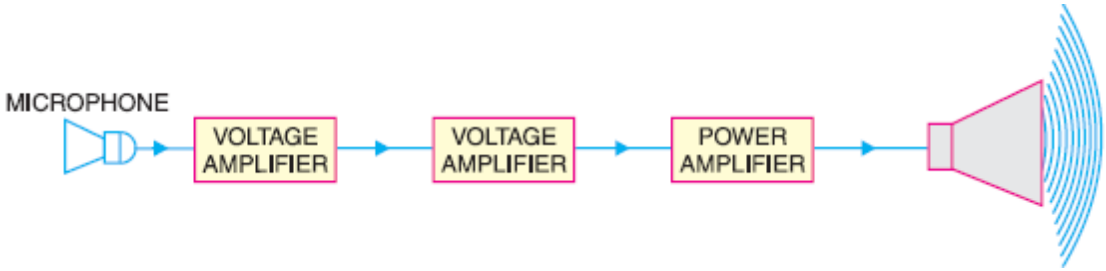
# Transistor Audio Power Amplifier

- A transistor amplifier which raises the power level of the signals that have audio frequency range is known as **transistor audio power amplifier.**
- A transistor that is suitable for power amplification is generally called a *power transistor*.
- The typical power output rating of a power amplifier is 1W or more.

# *Factors to be considered in large signal amplifiers:*

- Output power
- Distortion
- Operating region
- Thermal considerations
- Efficiency $(\eta)$

block diagram of an audio amplifier



# Difference Between Voltage and Power Amplifiers

| S. No. | Particular | Voltage amplifier | Power amplifier |
|---|---|---|---|
| 1. | β | High (> 100) | low (5 to 20) |
| 2. | $R_C$ | High (4 – 10 kΩ) | low (5 to 20 Ω) |
| 3. | *Coupling* | usually $R - C$ coupling | Invariably transformer coupling |
| 4. | *Input voltage* | low (a few mV) | High ( 2 – 4 V) |
| 5. | *Collector current* | low (≃ 1 mA) | High ( > 100 mA) |
| 6. | *Power output* | low | high |
| 7. | *Output impedance* | High (≃ 12 kΩ) | low (200 Ω) |

# Performance Quantities of Power Amplifiers

### (*i*) Collector efficiency

*The ratio of a.c. output power to the zero signal power (i.e. d.c. power) supplied by the battery of a power amplifier is known as* **collector efficiency**.

### (*ii*) Distortion

*The change of output wave shape from the input wave shape of an amplifier is known as* **distortion.**

### (*iii*) Power dissipation capability

*The ability of a power transistor to dissipate heat is known as* **power dissipation capability.**

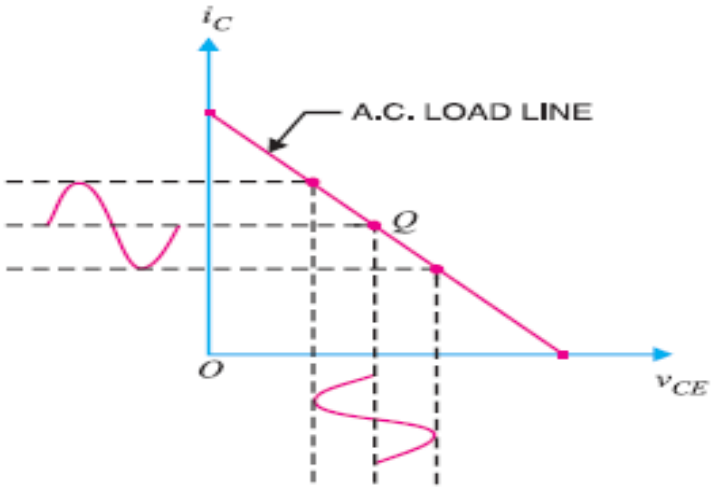
# Classification of Power Amplifiers

- Class A: It is one, in which the active device conducts for the full 360°.
- Class B: Conduction for 180 °.
- Class C: Conduction for < 180°.
- Class AB :Conduction angle is between 180°. and 360°.
- Class D: These are used in *transmitters because their efficiency is high: 100%.*
- Class S:Switching regulators are based on class'S' operation.

# Class A power amplifier

•If the collector current flows at all times during the full cycle of the signal, the power amplifier is known as **class A power amplifier.**

•If the Q point is placed near the centre a/the linear region a/the dynamic curve, class A operation results. Because the transistor will conduct for the complete 360 , distortion is low for small signals and conversion efficiency is low.



# Types of class-A power Amplifiers

## 1. Series fed

There is no transformer in the circuit. RL is in series with V cc. There is DC power drop across RL. Therefore efficiency = 25% (maximum).

## 2. Transformer coupled

- The load is coupled through a transformer. DC drop across the primary of the transformer is negligible. There is no DC drop across RL. Therefore efficiency = 50% maximum.

# Series Fed class-A power Amplifier

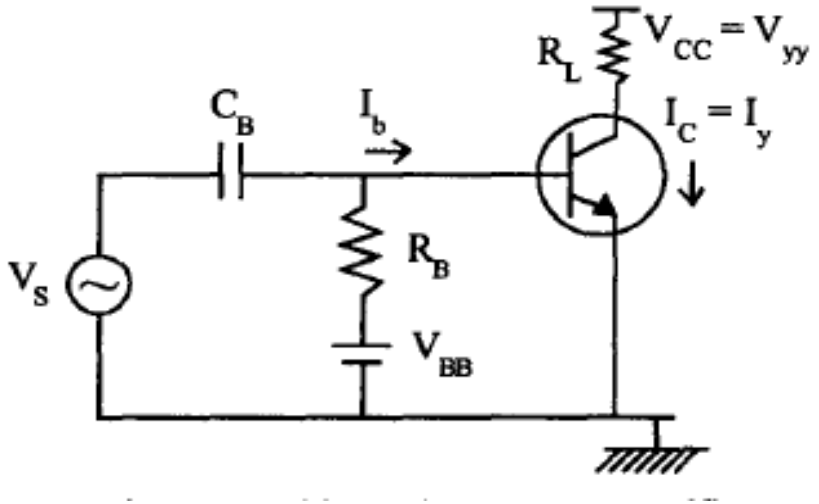



Fig.(a)Series fedClass A power amplifier circuit

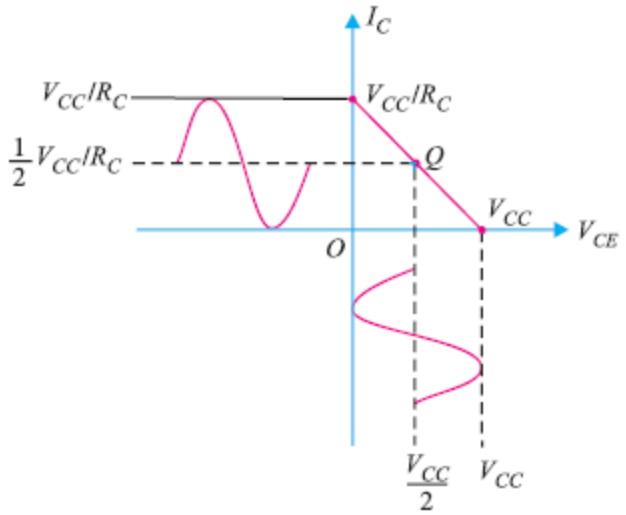



Fig.(b)Transter curve

# Transformer Coupled class-A power Amplifier

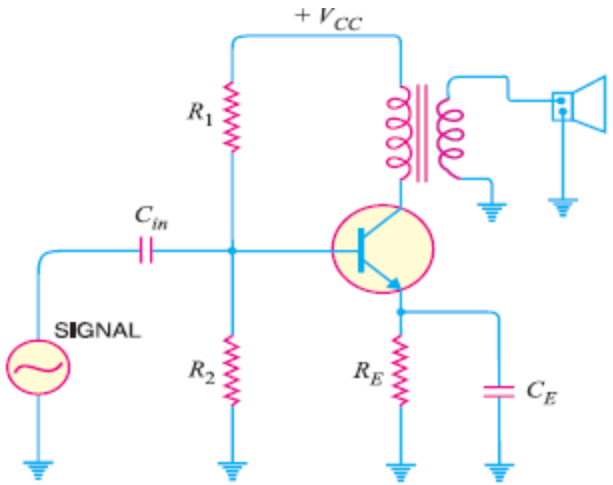



Fig.(a)Transformer Coupled Class A power amplifier circuit

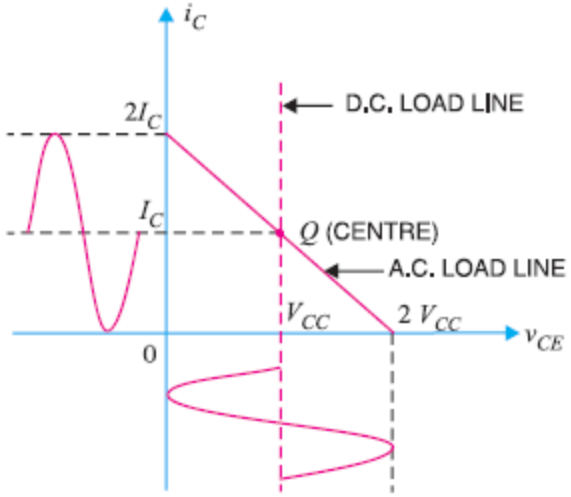



Fig.(b)Transfer curve

# Important Points About Class A Power Amplifier

- A transformer coupled class A power amplifier has a maximum collector efficiency of ***50%***
- The power dissipated by a transistor is given by :

$$P_{dis} = P_{dc} - P_{ac}$$

- When no signal is applied to a class *A power amplifier, Pac = 0.*

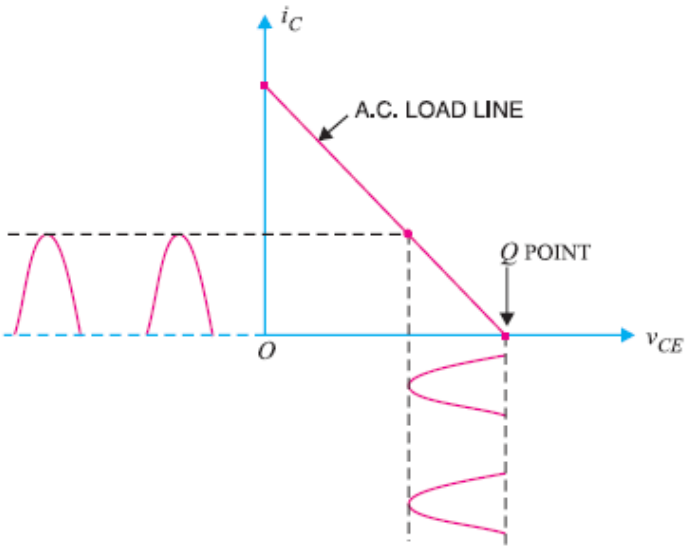
$$\therefore P_{dis} = P_{dc}$$

- When a class *A power amplifier is used in the final stage, it is called* ***single ended class A power amplifier.***

# Class B power amplifier

- If the collector current flows only during the positive half-cycle of the input signal, it is called a **class B power amplifier**.

•For class B operation the Q point is set near cutoff. So output power will be more and conversion efficiency is more. Conduction is only for 180




Transfer curve

# Types of class-B power Amplifiers

- **Push-Pull Amplifier**

  The standard class B push-pull amplifier requires a centre tapped transformer

- **Complimentary Symmetry Circuits (Transformer Less Class B Power Amplifier)**

  Complementary symmetry circuits need only one phase

  They don't require a centre tapped transformer.

# Advantages & Disadvantages of Class B power Amplifier

Advantages

1.More output power; efficiency = 78.5%. Max.

2.Efficiency is higher. Since the transistor conducts only for 180°, when it is not conducting, it will not draw DC current.

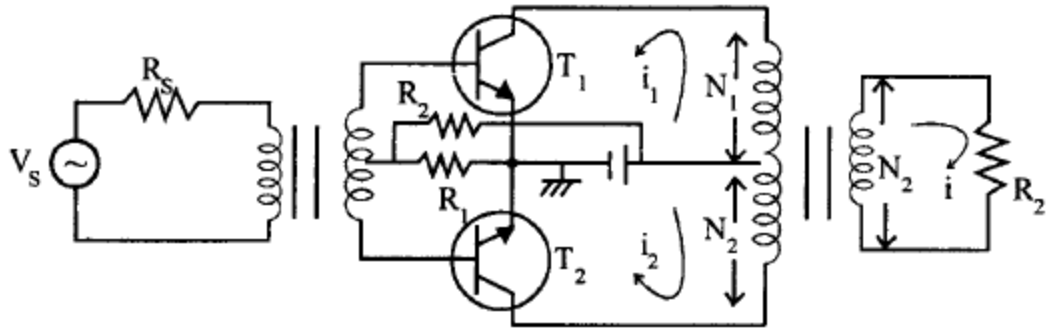
3. Negligible power loss at no signal.

Disadvantages:

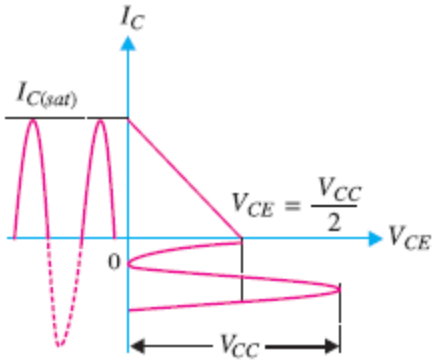
1. Supply voltage V cc should have good regulation. Since if V cc changes, the operating point changes (Since Ic changes). Therefore transistor may not be at cut off.

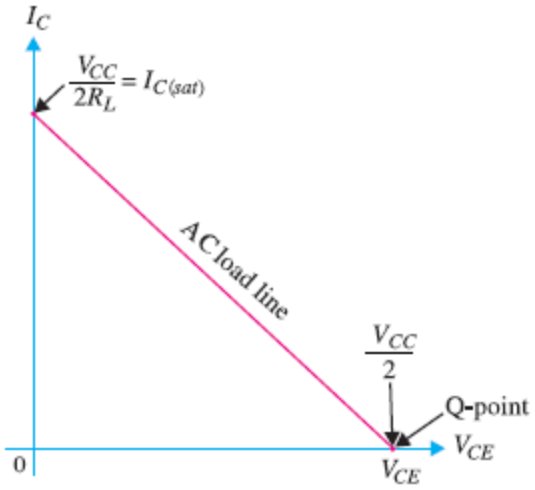
2. Harmonic distortion is higher. (This can be minimized by pushpull connection).

# Class B Push-Pull Amplifier




Push Pull amplifier circuit



# Complimentary Symmetry Circuits (Transformer Less Class B Power Amplifier)

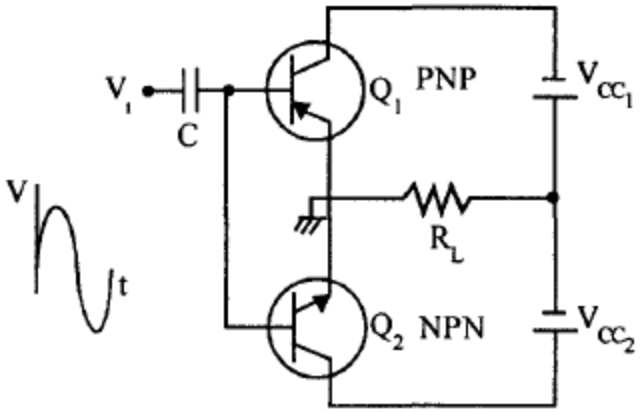



Fig. Complimentary Symmetry circuit

# Advantages & Disadvantages of Class B complementary power Amplifier

- **Advantages**

(i) This circuit does not require transformer. This saves on weight and cost.

(ii) Equal and opposite input signal voltages are not required.

- **Disadvantages**

(i) It is difficult to get a pair of transistors (npn and pnp) that have similar characteristics.

(ii) We require both positive and negative supply voltages.

# Differences between class-A & B power Amplifiers

| Class A | Class B |
| --- | --- |
| Less power | More power |
| Lesser $\eta$ | More $\eta$ upto 78.5% |
| Less Harmonic distortion | Harmonic distortion is more |

# Heat Sinks

•The metal sheet that serves to dissipate the additional heat from the power transistor is known as **heat sink.**

•The purpose of heat sinks is to keep the operating temperature of the transistor low, to prevent thermal breakdown.

•Almost the entire heat in a transistor is produced at the collector-base junction. If the temperature exceeds the permissible limit, this junction is destroyed and the transistor is rendered useless.

• Most of power is dissipated at the collector-base junction. This is because collector-base voltage is much greater than the base-emitter voltage, although currents through the two junctions are almost the same.

# Mathematical Analysis Of Heat Sinks

$$\theta_{ja} = \theta_{jc} + \theta_{cn} + \theta_{na}$$

$$\theta_{jc} = (T_j - T_c) / P$$

$$\theta_{cs} = (T_c - T_s) / P$$

$$\theta_{sa} = (T_s - T_a) / P$$

$\theta_{ja}$ = Junction to ambient thermal resistance

$\theta_{jc}$ = Junction to casing thermal resistance

$\theta_{cs}$ = Casing to heat sink thermal resistance

$\theta_{sa}$ = Heat sink to ambient thermal resistance

$T_j$ = Average junction temperature

$T_c$ = Average case temperature

$T_{sa}$ = Average heat sink temperature

$T_a$ = Ambient temperature

$P$ = Power dissipated in Watts.

# Classification of heat Sinks

1. Low Power Transistor Type.

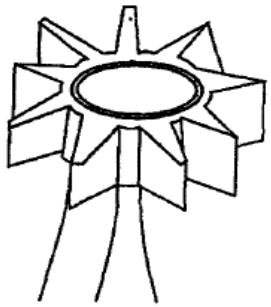
2. High Power Transistor Type.

# Low Power Transistor Type.

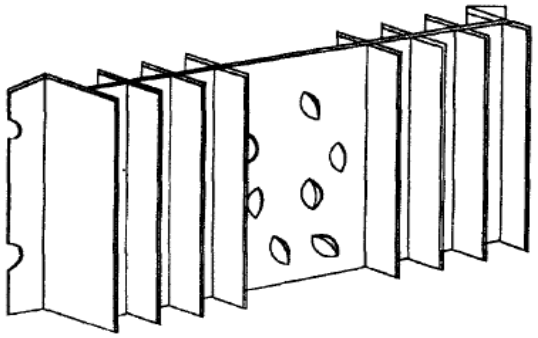
- Low Power Transistors can be mounted directly on the metal chassis to increase the heat dissipation capability. The casing of the transistor must be insulated from the metal chassis to prevent shorting.
- Beryllium oxide insulating washers are used for insulating casing from the chassis. They have good thermal conductivity.
- Zinc oxide film silicon compound between washer and chassis, improves the heat transfer from the semiconductor device to case to the chassis.

# High Power Transistor Type.

- re TO-3 and TO-66 types. These are diamond shaped. For power transistors, usually, the ease itself in the collector convention and radiation
- Finned aluminium heat sinks yield the best heat transfer per unit cost.



Fin-type heat sink



Power transistor heat sink

# Alternate Methods to prevent Thermal breakdown

- It should be realized that the use of heat sink alone may not be sufficient to prevent thermal runaway under all conditions. In designing a transistor circuit, consideration should also be given to the choice of

(*i)* operating point

(ii) ambient temperatures which are likely to be encountered and

(iii)the type of transistor e.g. metal case transistors are more readily cooled by conduction than plastic ones.

# Tuned Amplifiers

•Amplifiers which amplify a specific frequency or narrow band of frequencies are called **tuned amplifiers.**

•Tuned amplifiers are mostly used for the amplification of high or radio frequencies.

• It offers a very high impedance at *resonant frequency* and very small impedance at all other frequencies.

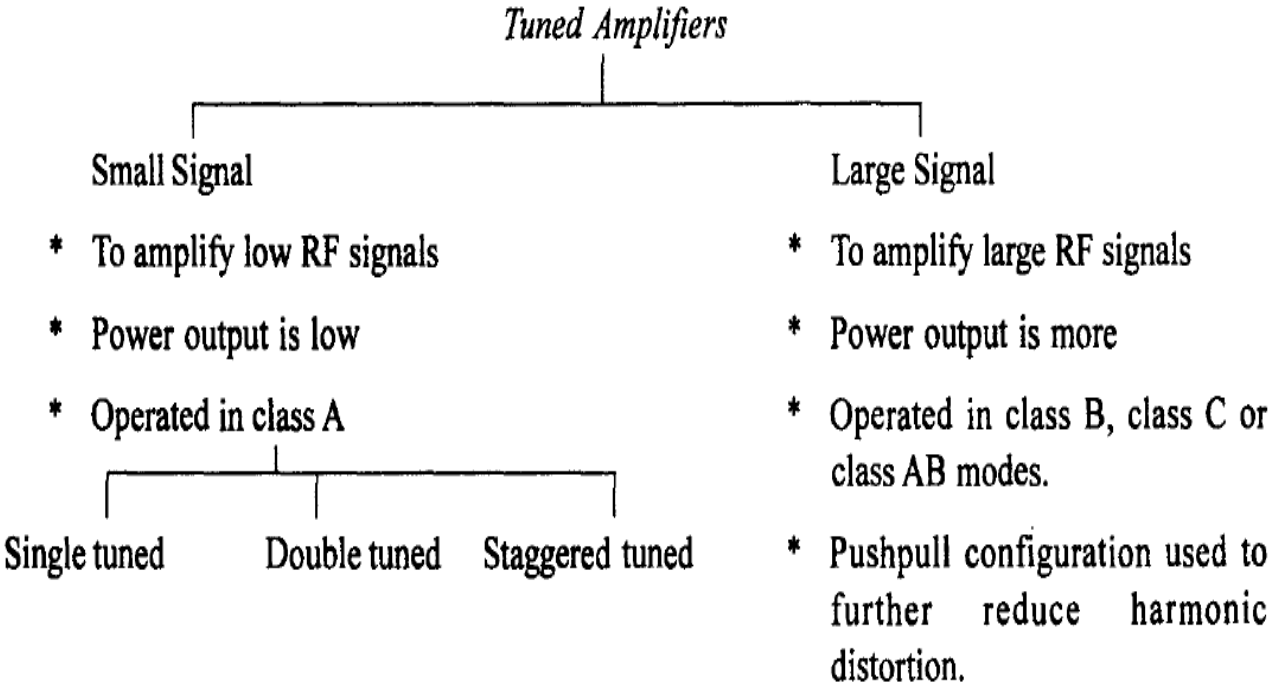
# Advantages of Tuned Amplifiers

1. **Small power loss.**
2. **High selectivity**
3. **Smaller collector supply voltage**
4. **Used in RF amplifiers, Communication receivers, Radar , Television ,I.F amplifiers**
5. **harmonic distortion is very small**

# Why not Tuned Circuits for Low Frequency Amplification?

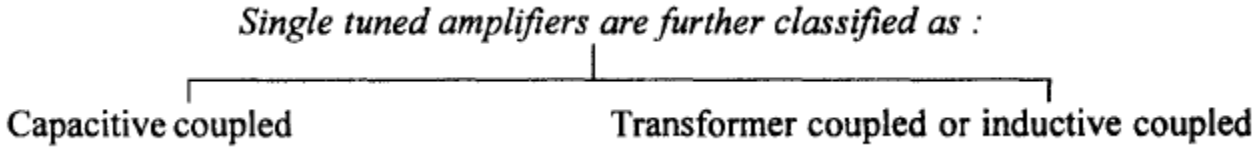
- *Low frequencies are never single*
- *High values of L and C*.

# Classification

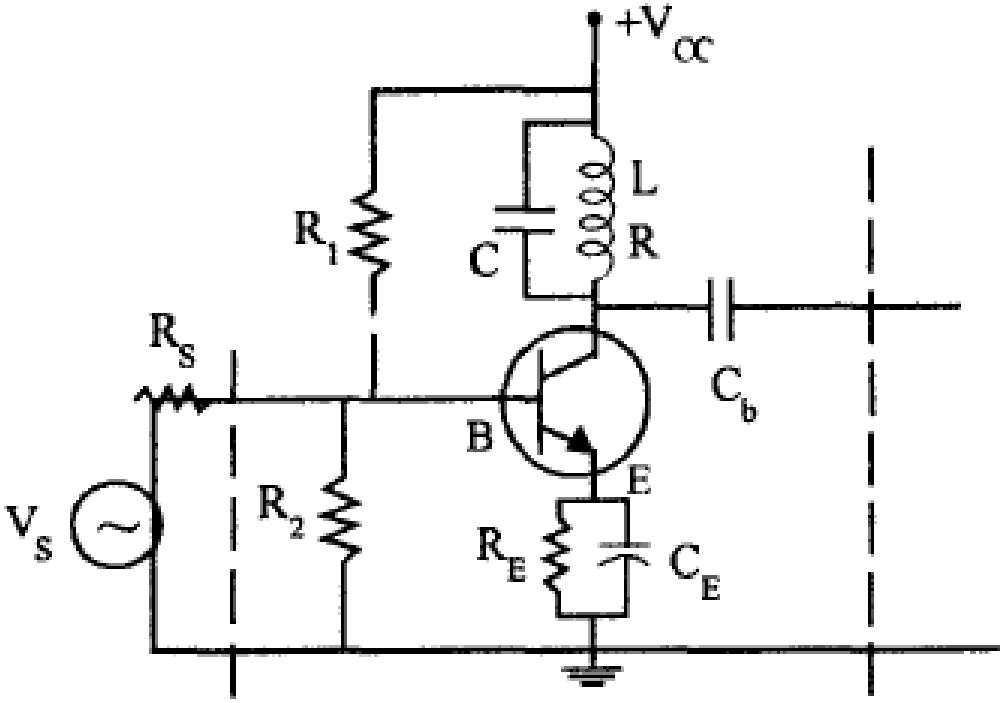


# Single Tuned Amplifier

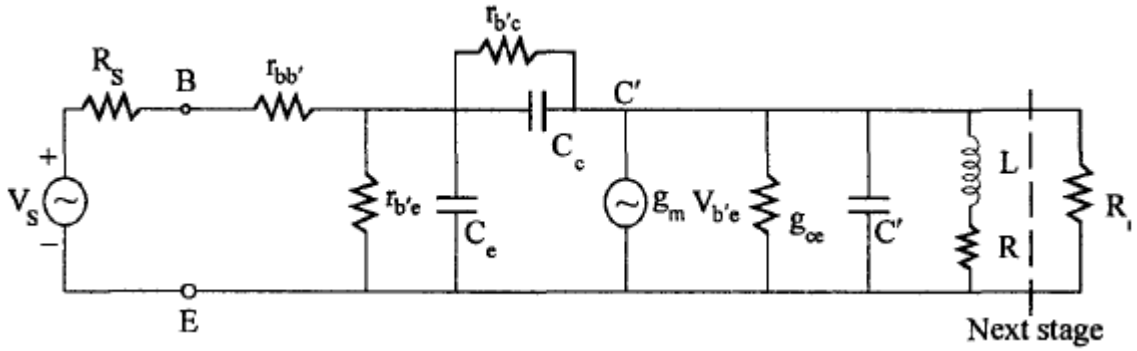
•Uses one parallel tuned circuit as the load IZI in each stage and all these tuned circuits in different stages are tuned to the same frequency. To get large Av or Ap, multistage amplifiers are used. But each stage is tuned to the same frequency, one tuned circuit in one stage.



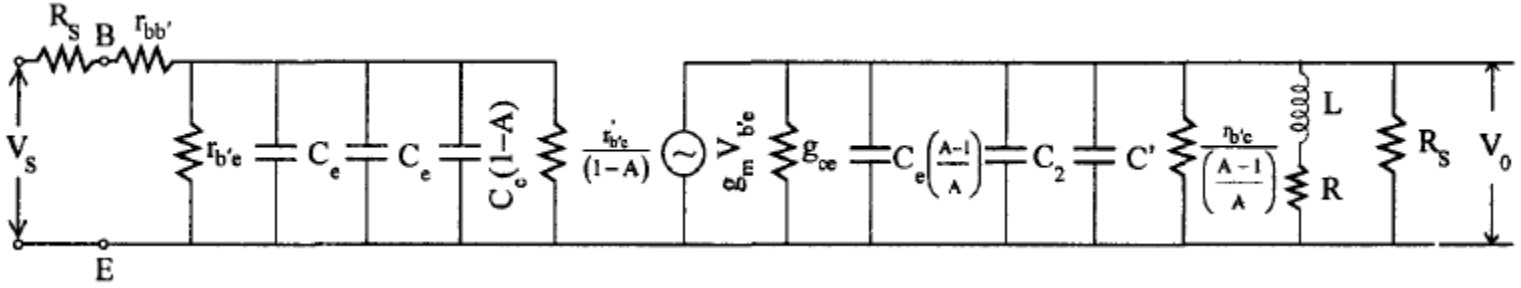
# Single Tuned Capacitive Coupled Amplifier



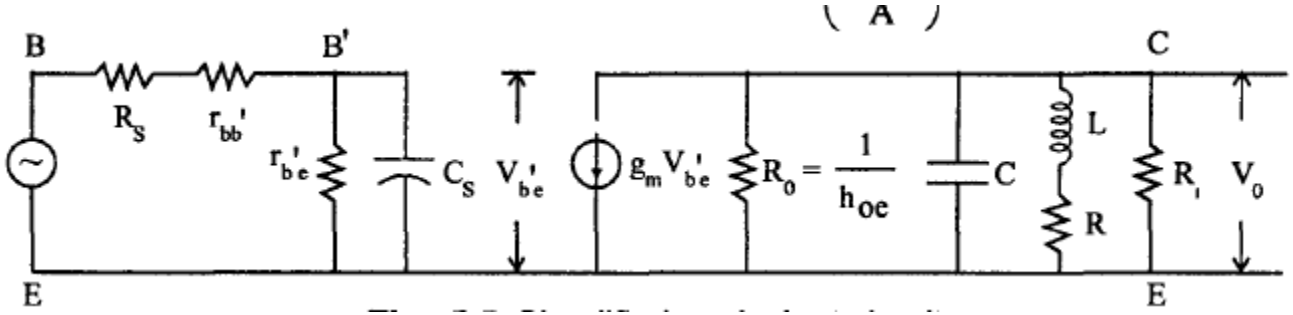
# Equivalent circuit of Single Tuned Capacitive Coupled Amplifier



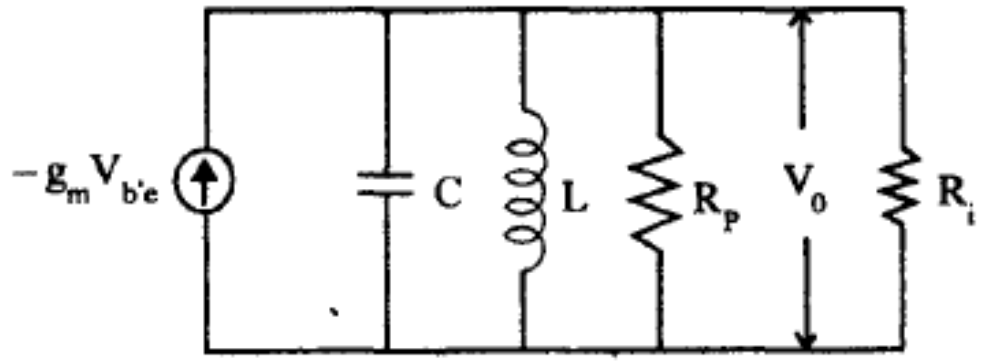
# Equivalent circuit of Single Tuned Capacitive Coupled Amplifier(applying Miller's Theorem)



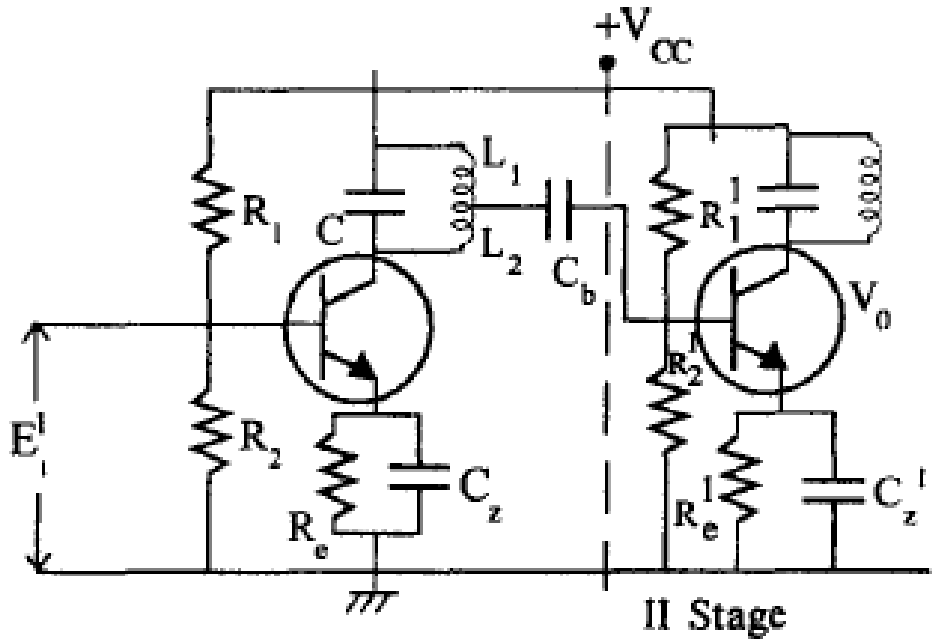
# Simplified equivalent circuit



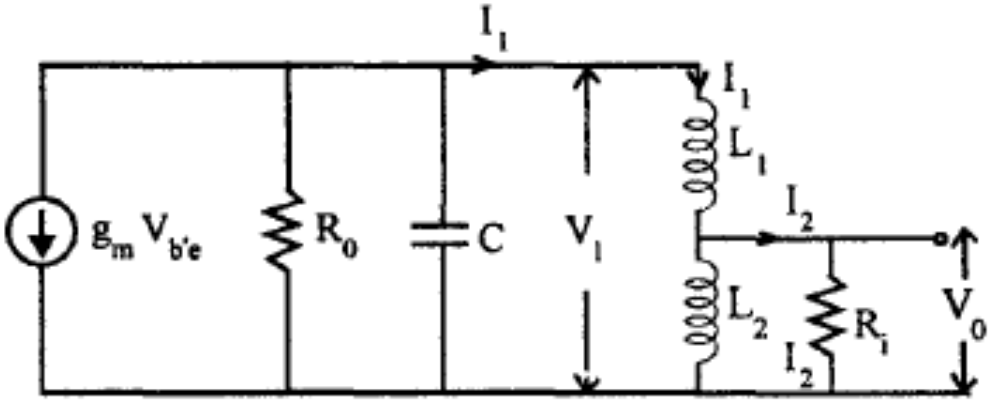
# Simplified output circuit



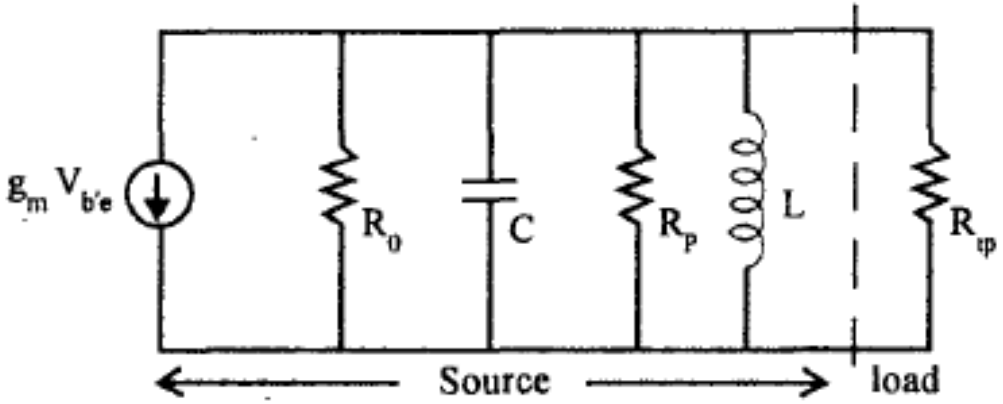
# Tapped Single Tuned Capacitance Coupled Amplifier



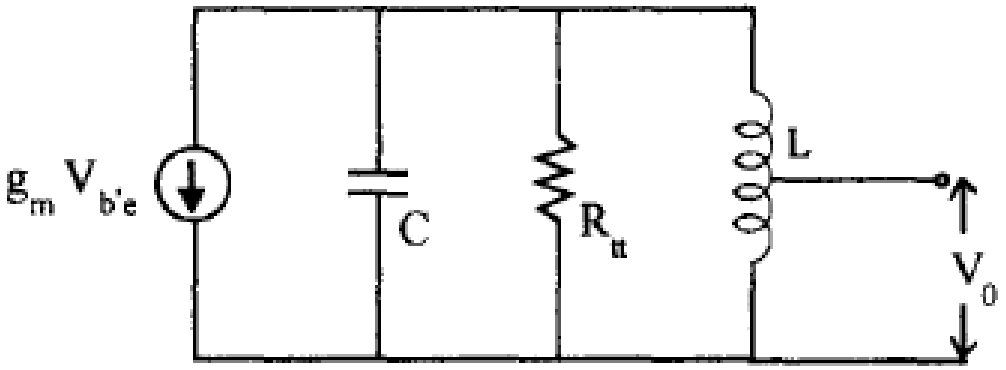
# Equivalent Circuit on the Output Side of the I Stage



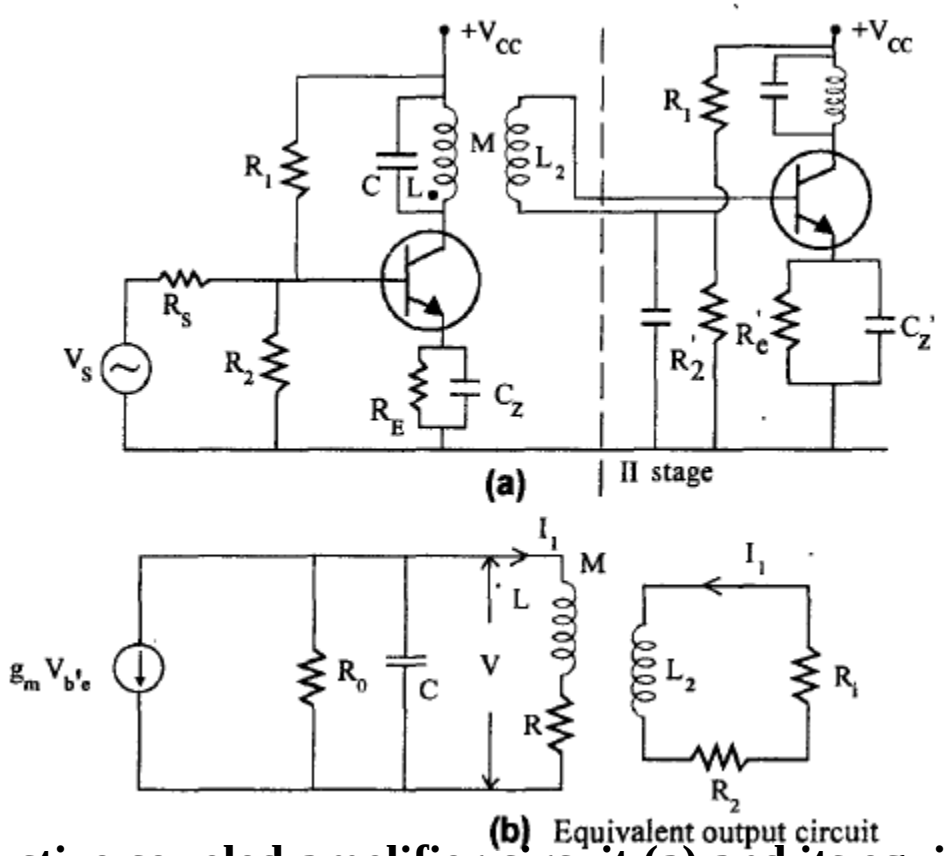
# Equivalent circuit of Tapped Single Tuned Capacitance Coupled Amplifier



# Equivalent circuit after simplification

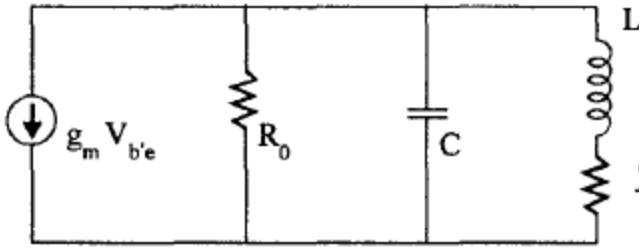


# Single Tuned Transformer Coupled or Inductively Coupled Amplifier

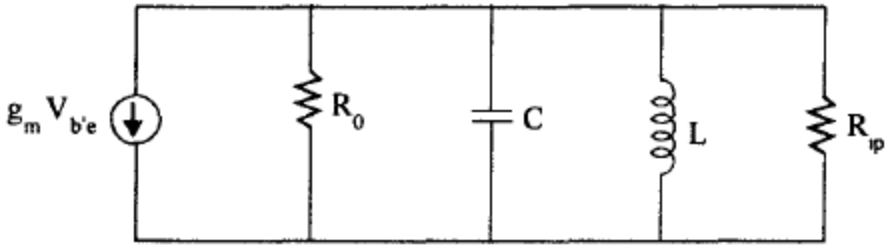



**Inductive coupled amplifier circuit (a) and its equivalent (b)**

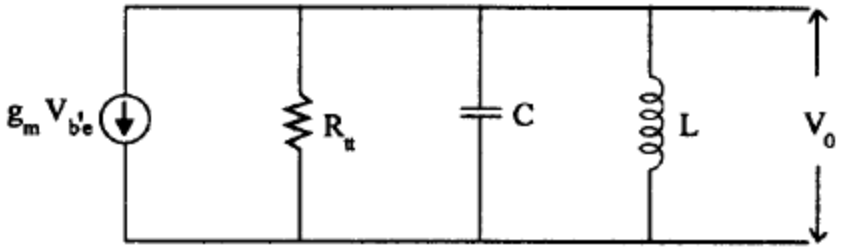
# Single Tuned Transformer Coupled or Inductively Coupled Amplifier




(a)Equivalent circuit




(b)Simplified circuit

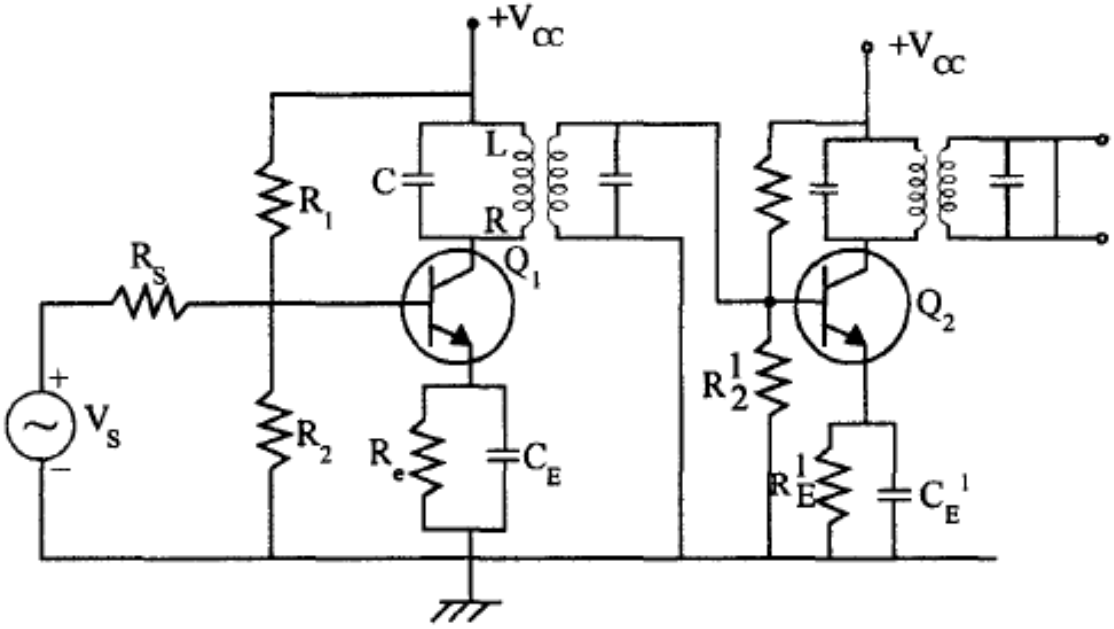



©Equivalent circuit

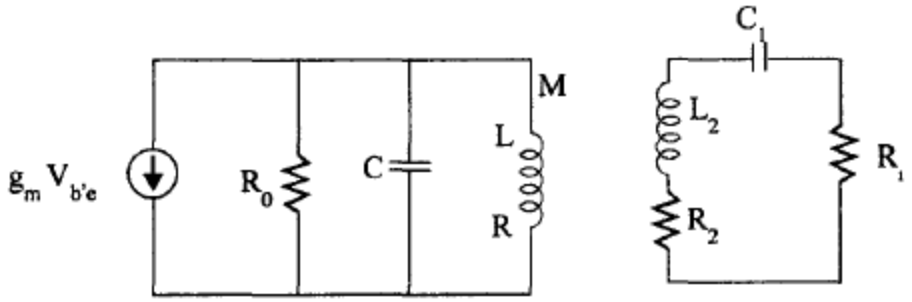
# Double Tuned Amplifier

- It uses two inductively coupled tuned circuits, for each stage of the amplifier. Both the tuned circuits are tuned to the same frequency, two tuned circuits in one stage, to get sharp response.
- It provides larger 3-db band width than the single tuned amplifier. Therefore Gain x Bandwidth product is more.
- It provides gain - frequency curve having steeper sides and flatter top.

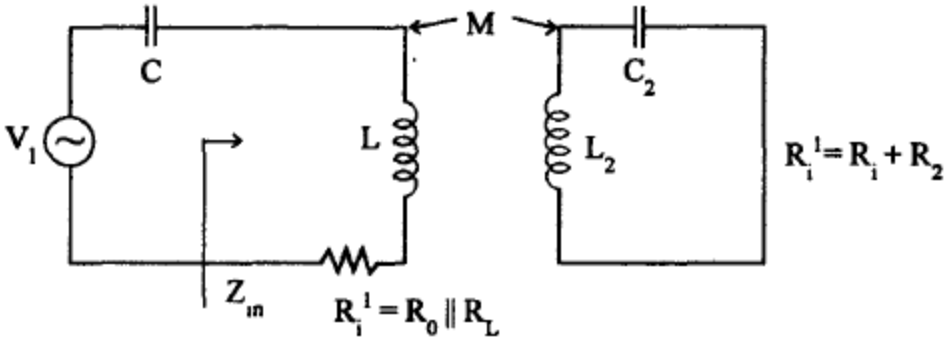
# Double tuned amplifier circuit



# Double tuned amplifier Equivalent circuit



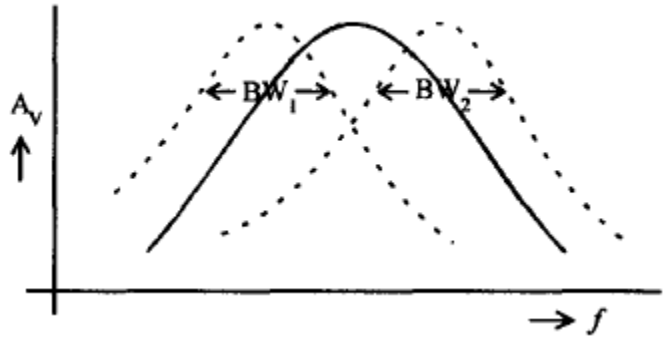

(a)Equivalent circuit




(b)Modified circuit

# Stagger Tuned Amplifier

**•This circuit uses number of single tuned stages in cascade. The successive tuned circuits are tuned to slightly different frequencies.**




Variation of Av with f

# Stability Considerations

- Thermal Effects
- Bias Considerations: Distortion in Audio amplifiers and other types of circuits depends on :

  (i) Input signal level (in mv)

  (ii) Source Resistance

  (iii) Bias Conditions

  (iv) Type of output load and its impedance

  (v) Loading effect.

## Relation between hybrid-$\pi$ and h-parameters

| Sr. No | Parameter Relation |
|---|---|
| 1 | $g_m = \frac{I_C}{V_T}$ |
| 2 | $r_{b'e} = \frac{h_{fe}}{g_m}$ |
| 3 | $r_{bb'} = h_{ie} - r_{b'e}$ |
| 4 | $r_{b'c} = \frac{r_{b'e}}{h_{re}}$ |
| 5 | $g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_{b'c}\, h_{fe}$ |

# Hybrid - *n Parameter Values*

Typical values of the hybrid-π parameter at $I_C$ = 1.3 mA are as follows :

$g_m$ = 50 mA/V  $r_{bb'}$ = 100 Ω  $r_{b'e}$ = 1 kΩ

$r_{ce}$ = 80 kΩ  $C_c$ = 3 pf  $C_e$ = 100 pf

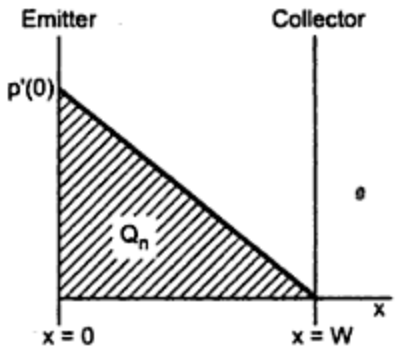
$r_{b'c}$ = 4 MΩ

*These values depend upon :*

1. Temperature
2. Value of $I_C$

## The Hybrid-$\pi$ Capacitances

$$C_e = C_{De} + C_{Te} \approx C_{De}$$




$$Q_B = \frac{1}{2} P'(0)\, A\, W\, q$$

$$I = -Aq\, D_B \frac{dp'}{dx}$$

$$= Aq\, D_B \frac{p'(0)}{W}$$

Combining equations (1) and (2) we get

$$Q_B = \frac{IW^2}{2\, D_B}$$

$$C_{De} = \frac{d\, Q_B}{dV} = \frac{W^2}{2\, D_B} \frac{dI}{dV}$$

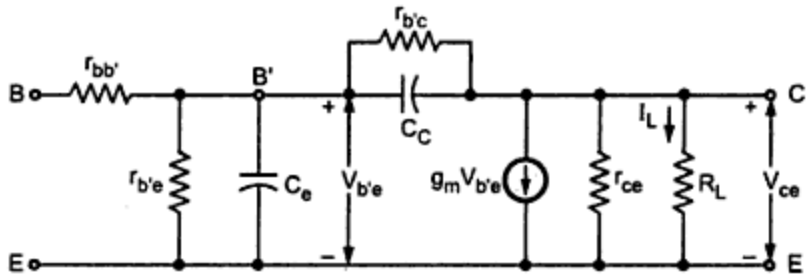
$$= \frac{W^2}{2\, D_B} \frac{I}{r_e}$$

$r_e = dV/dI = V_T/I_E$ is the emitter junction incremental resistance.

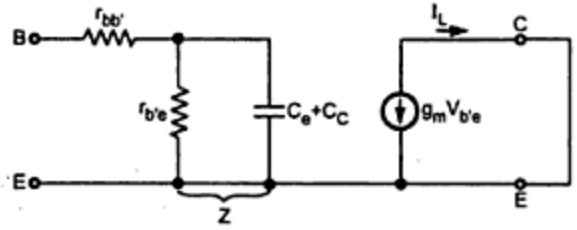
$$C_{De} = \frac{W^2 I_E}{2 D_B V_T} = g_m \frac{W^2}{2 D_B}$$

$$C_e \approx \frac{g_m}{2\pi f_T}$$

## CE Short-Circuit Current Gain using Hybrid $\pi$ Model

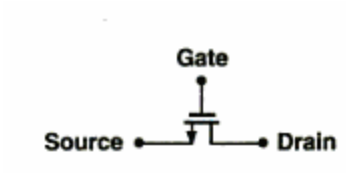



**The hybrid-$\pi$ circuit for a single transistor with a resistive load $R_L$**

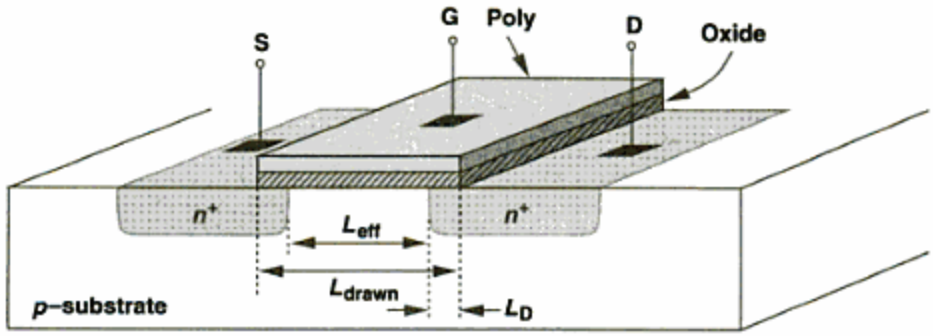


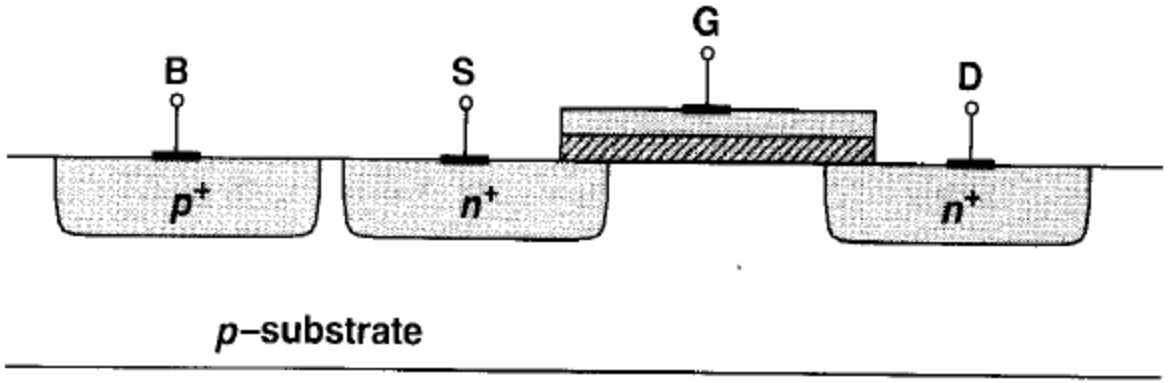

**Simplified hybrid-$\pi$ model for short circuit CE transistor**

Simple view of a MOS

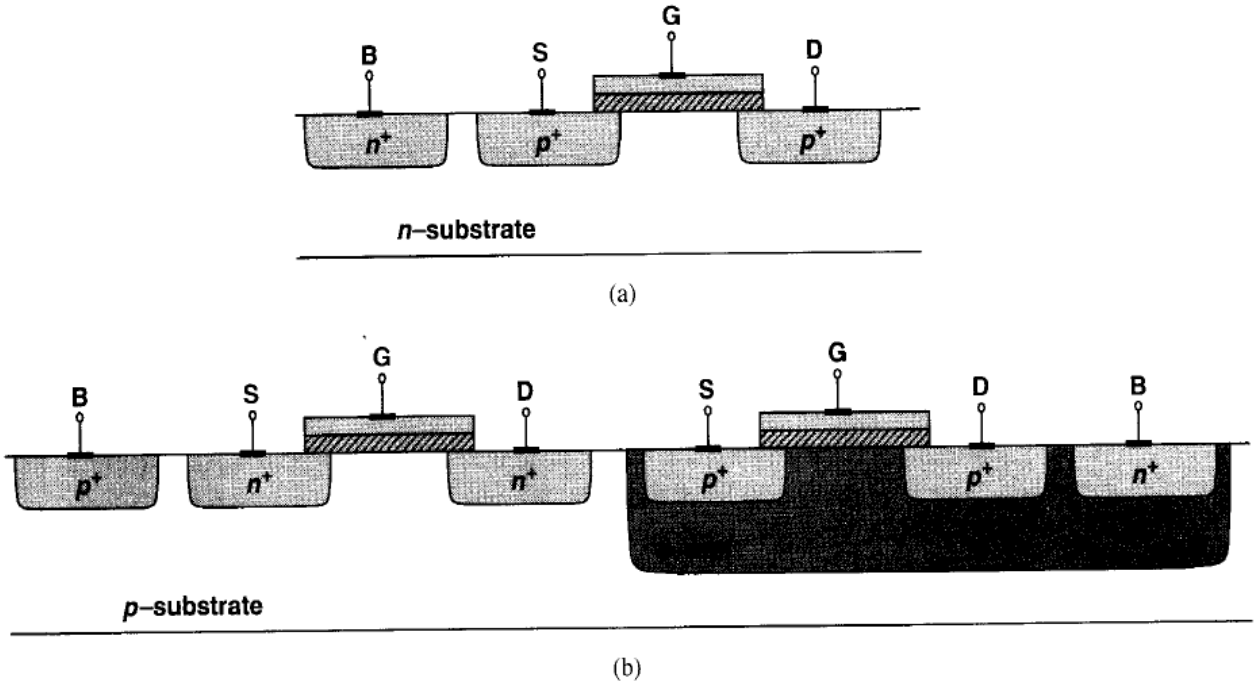



**MOSFET Structure**



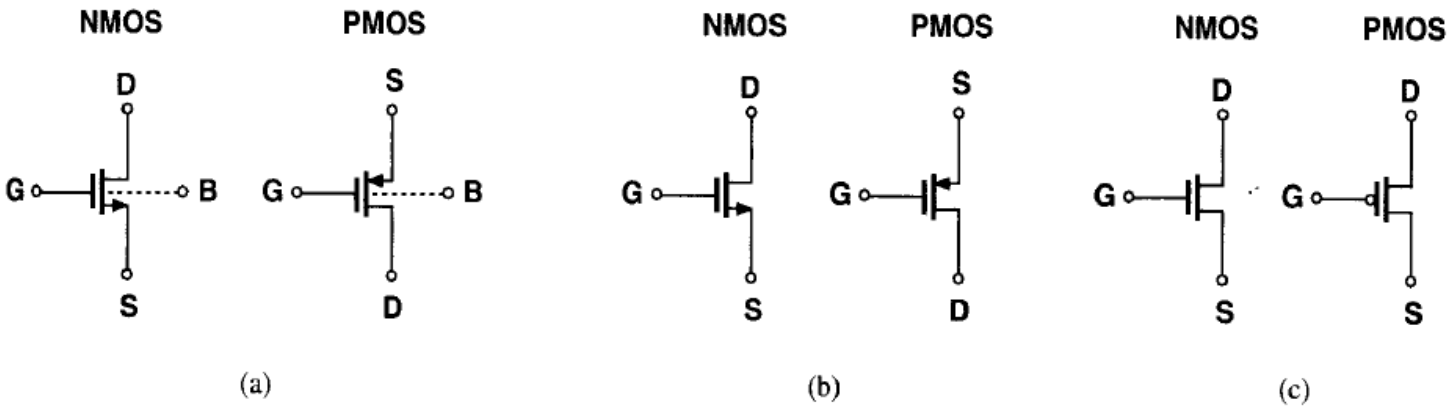



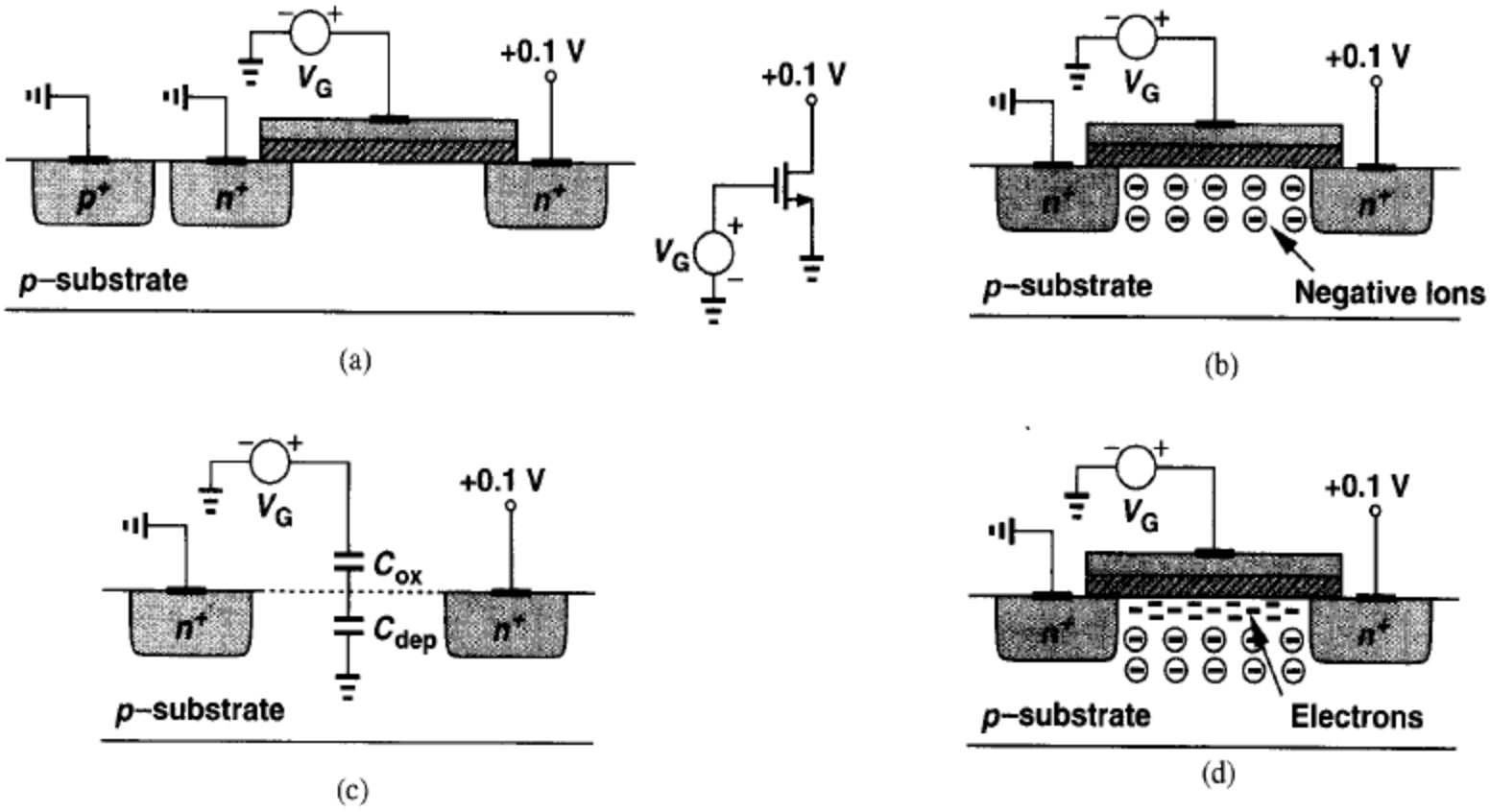

Substrate connection.




(a) Simple PMOS device, (b) PMOS inside an $n$-well.

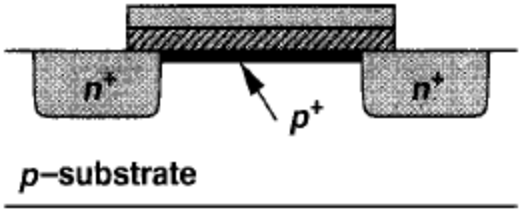
MOS symbols.



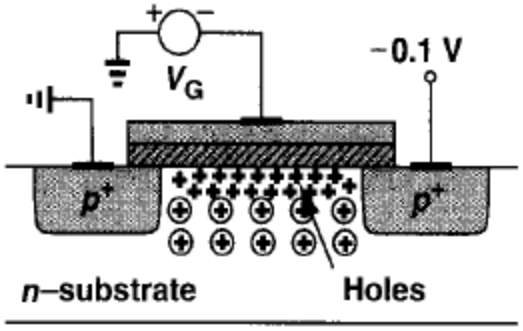


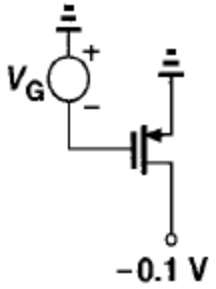

(a) A MOSFET driven by a gate voltage, (b) formation of depletion region, (c) onset of inversion, (d) formation of inversion layer.

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}},$$




Implantation of $p^+$ dopants to alter the threshold.

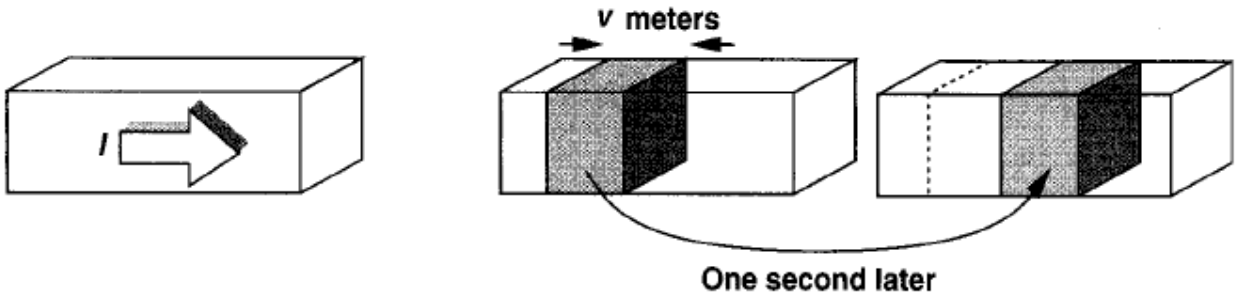



Formation of inversion layer in a PFET.

## Derivation of I/V Characteristics

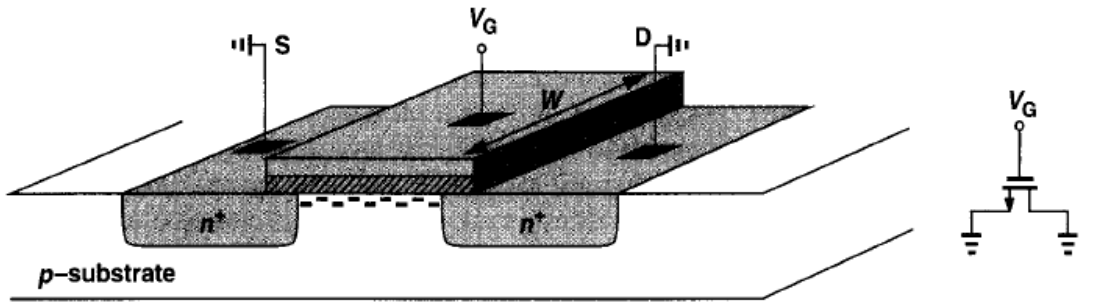
$$I = Q_d \cdot v.$$



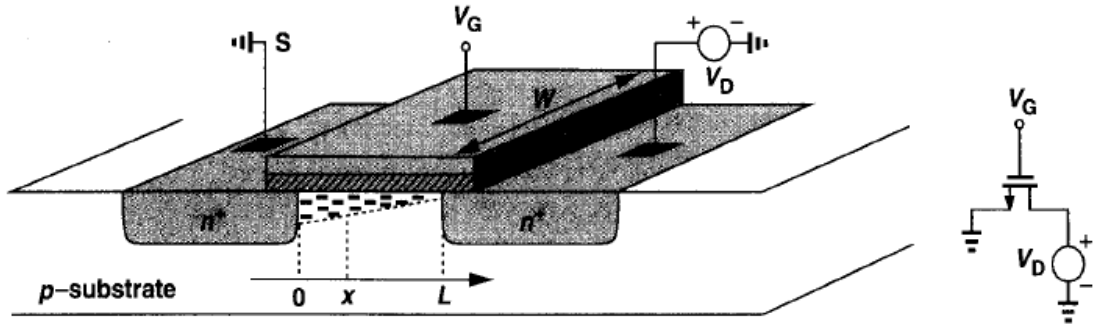

(a) (b)

(a) A semiconductor bar carrying a current $I$, (b) snapshots of the carriers one second apart.

Channel charge with (a) equal source and drain voltages, (b) unequal source and drain voltages.

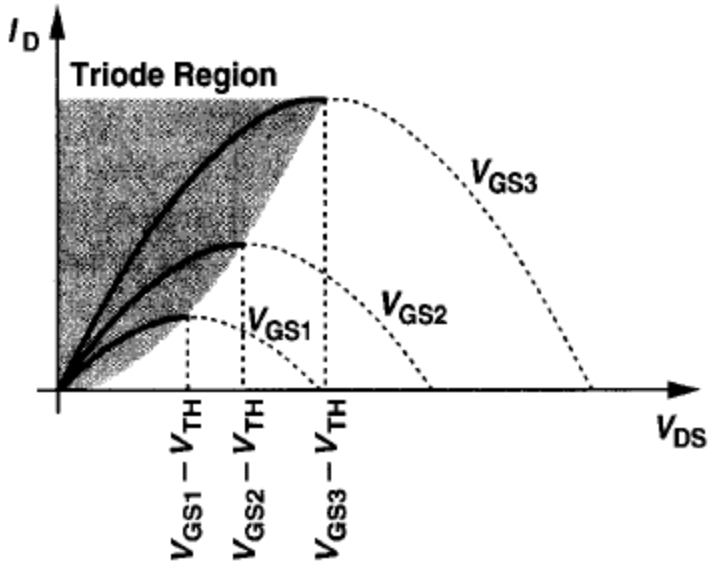



(a)




(b)

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx},$$

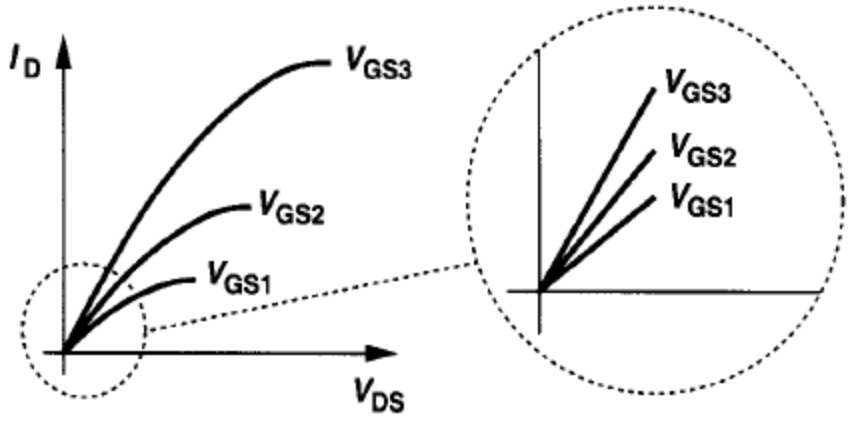



Drain current versus drain-source voltage in the triode region.

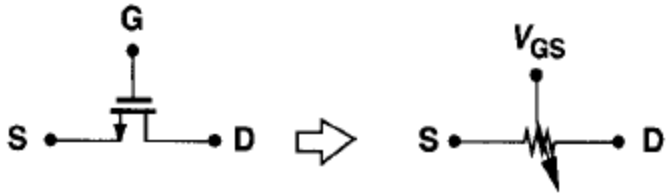
$$I_{D,max} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2.$$

$$I_D \approx \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS},$$

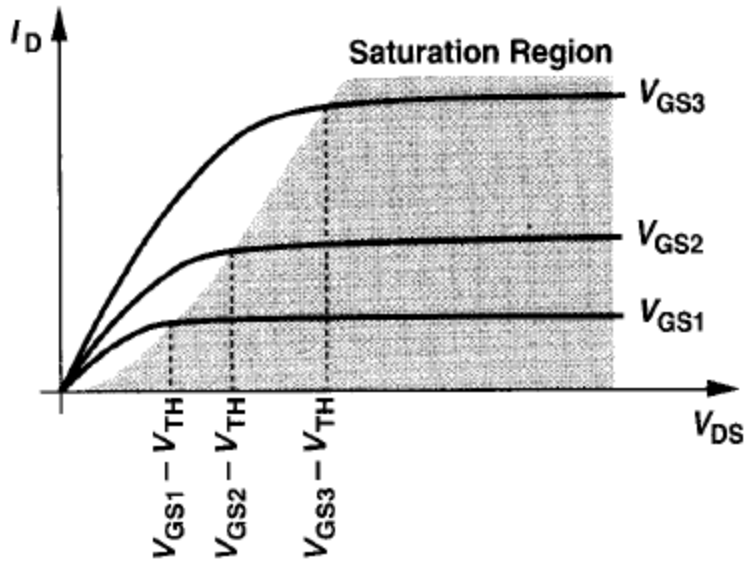
$$R_{on} = \frac{1}{\mu_n C_{ox}\dfrac{W}{L}(V_{GS} - V_{TH})}.$$



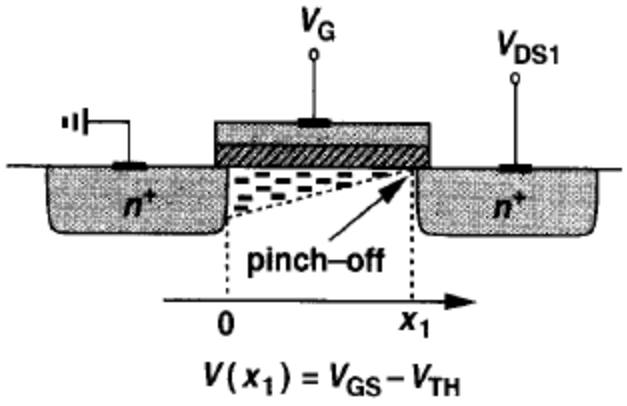

Linear operation in deep triode region.

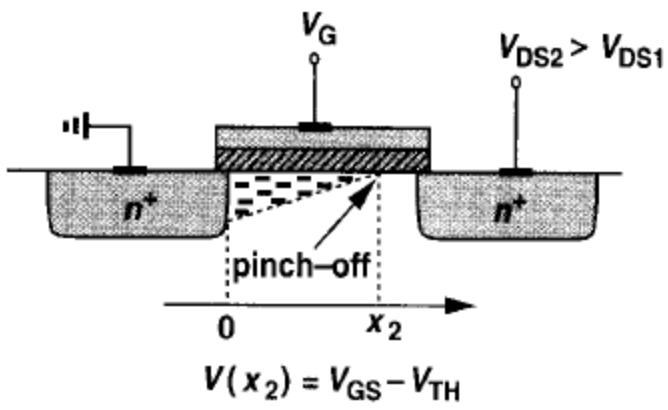



With the condition $V_{DS} \ll 2(V_{GS} - V_{TH})$, we say the device operates in deep triode region.




Saturation of drain current.



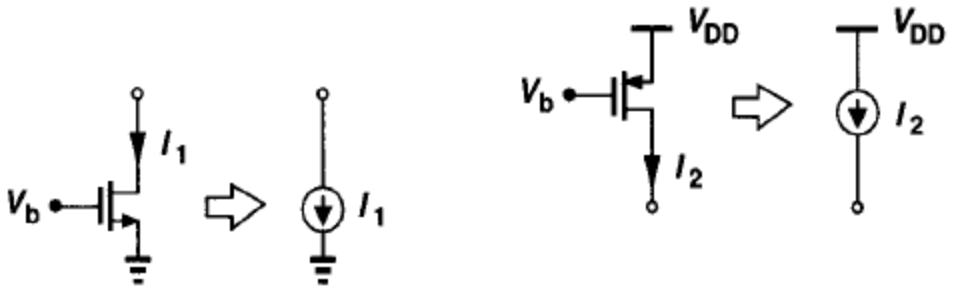




Pinch-off behavior.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2,$$

$$I_D = -\mu_p C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2.$$

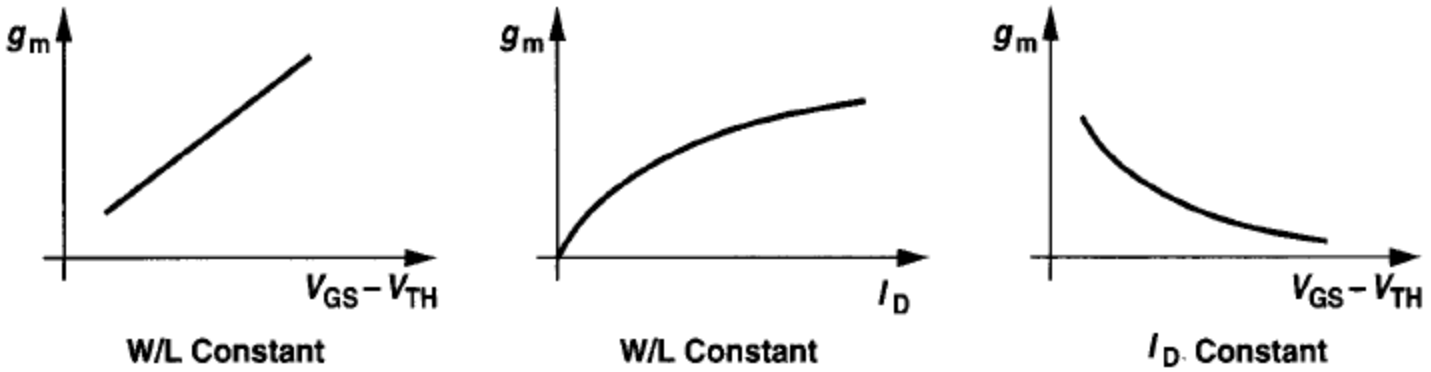



Saturated MOSFETs operating as current sources.

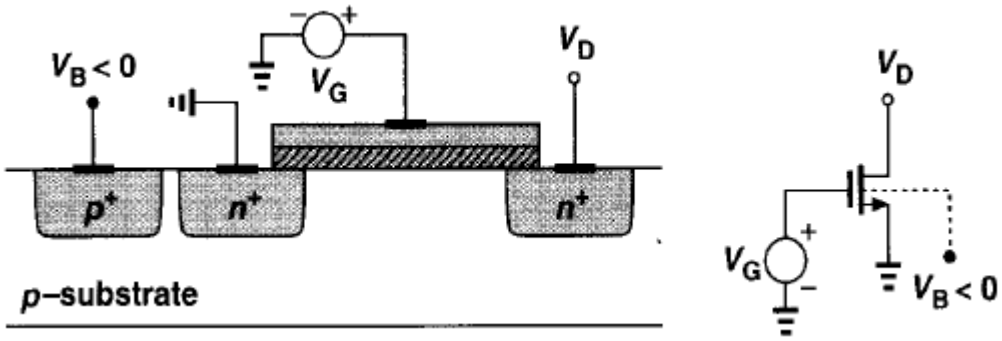
$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS,\text{const.}}$$
$$= \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}).$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$
$$= \frac{2I_D}{V_{GS} - V_{TH}}.$$

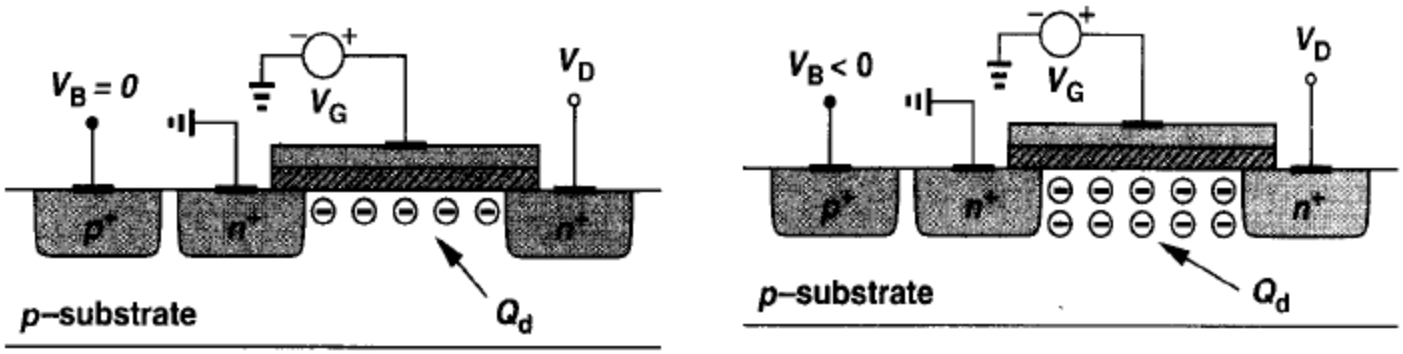
MOS transconductance as a function of overdrive and drain current.



NMOS device with negative bulk voltage.

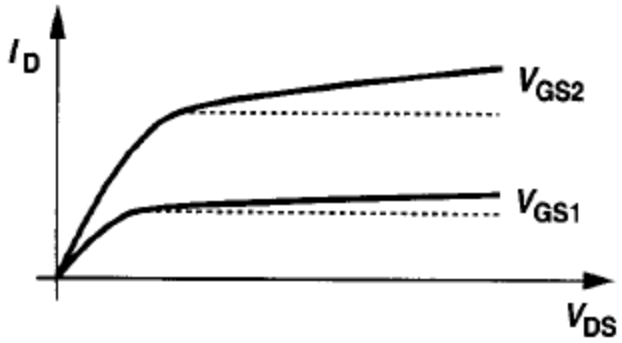


Variation of depletion region charge with bulk voltage.




## Channel-Length Modulation

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}),$$



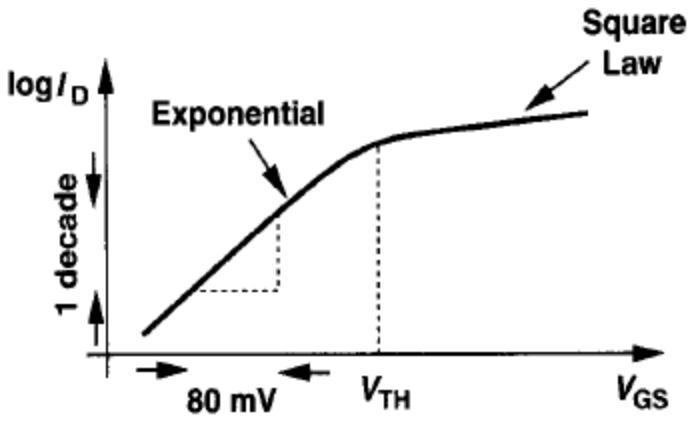

Finite saturation region slope resulting from channel-length modulation.

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}).$$

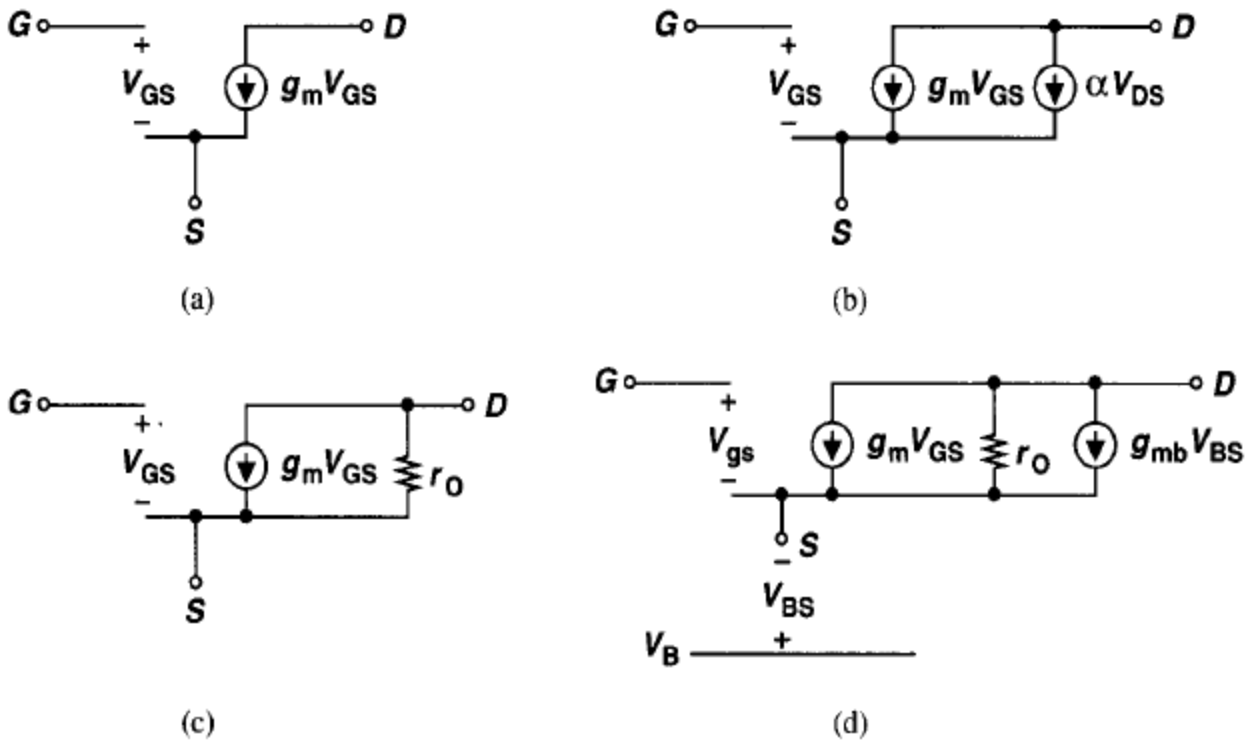
$$= \sqrt{\frac{2\mu_n C_{ox}(W/L) I_D}{1 + \lambda V_{DS}}},$$

## Subthreshold Conduction

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_T},$$




MOS subthreshold char-

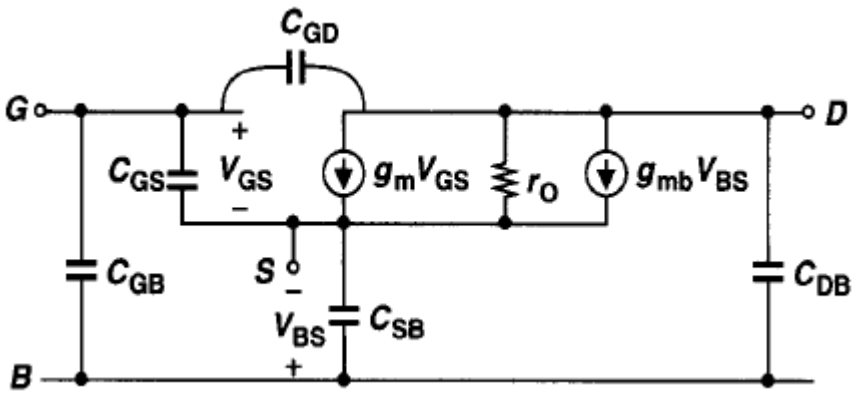



(a) Basic MOS small-signal model, (b) channel-length modulation represented by a dependent current source, (c) channel-length modulation represented by a resistor, (d) body effect represented by a dependent current source.

$$
\begin{aligned}
r_O &= \frac{\partial V_{DS}}{\partial I_D} \\
&= \frac{1}{\partial I_D / \partial V_{DS}}. \\
&= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \cdot \lambda} \\
&\approx \frac{1}{\lambda I_D}.
\end{aligned}
$$

$$
\begin{aligned}
g_{mb} &= g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} \\
&= \eta g_m,
\end{aligned}
$$

Complete MOS small-signal model.



**Code No: 124CV** **R15**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, April - 2018**
**ELECTRONIC CIRCUIT ANALYSIS**
**(Common to ECE, EIE, ETM)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

**PART- A**

**(25 Marks)**

| | | |
|---|---|---|
| 1.a) | Draw the circuit diagram of Darlington Pair. | [2] |
| b) | What is the expression for harmonic distortion in single stage amplifiers? | [3] |
| c) | Define Gain-Bandwidth Product in detail. | [2] |
| d) | Draw the Small signal model of MOS amplifier. | [3] |
| e) | List out the Conditions for Oscillations in detail. | [2] |
| f) | Explain different Classification of Feedback Amplifiers. | [3] |
| g) | Define Thermal Stability and Thermal Runway. | [2] |
| h) | What is Heat sink and explain its advantages? | [3] |
| i) | Define Q factor. | [2] |
| j) | What is the expression for harmonic distortion in tuned amplifiers? | [3] |

**PART-B**

**(50 Marks)**

2.a) Discuss about effect of Cb on frequency response of RC coupled amplifier.
b) Draw the circuit diagram of Direct Coupled Amplifier and explain its operation in detail. [5+5]

**OR**

3.a) With a neat circuit diagram. Explain about Boo-Strap emitter follower amplifier.
b) Derive the Analysis of CE amplifier with Emitter Resistance and explain its operation along with circuit diagram. [5+5]

4.a) Find the voltage gain, input and output resistances of a emitter follower at high Frequencies.
b) A common source amplifier uses a MOSFET with the following parameters gm=1.5mA/V, rd=40kohms, Cgs=3pF, Cds=1pF, Cgd=3.2pF. The value of Rd=200Kohms. The amplifier operates at 30KHz. Find Voltage gain, input resistance, output resistance and input capacitance. [5+5]

**OR**

5.a) Draw the circuit diagram of Common source amplifier with Resistive load and explain its operation.
b) Derive the expression for $f_T$ of a transistor in detail. [5+5]

6.a) Derive the expression for frequency of oscillation of BJT RC phase-shift oscillator with necessary explanation.

b) What is the equivalent circuit of a crystal? Derive the expressions for series and parallel resonances. A crystal oscillator has the following parameters: L=0.33H, C=0.065pF, Cm=1.0pF and R=5.5 k ohm.
i) Find the series resonant frequency.
ii) Find the Q of the crystal. [5+5]

**OR**

7.a) Draw the block diagrams of four types of negative feedback amplifier circuits and explain the advantages and disadvantages with necessary derivations.

b) Explain why RC Phase shift oscillators are not used at high frequencies. [5+5]

8.a) Explain the operation of a class A push-pull power amplifier and list out its advantages and disadvantages.

b) A single transistor is operating as an ideal class B amplifier with a 10-K load. A dc meter in the collector circuit reads 8mA. How much signal power is delivered to the load? [5+5]

**OR**

9.a) Draw the circuit diagram of Complementary Symmetry Class B Push-Pull Amplifier and explain its operation.

b) List out the few difference between Class A, Class B and Class AB Push-Pull amplifiers with examples. [5+5]

10.a) What is a stagger tuned amplifier? Explain its advantages and disadvantages.

b) Write short notes on Small Signal Tuned Amplifiers in detail. [5+5]

**OR**

11.a) What are the different Effect of Cascading Single Tuned Amplifiers on Bandwidth in detail.

b) Explain the concept of Stability of Tuned Amplifiers with one example. [5+5]

**---ooOoo---**

**Code No: 124CV** **R15**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, May - 2017**
**ELECTRONIC CIRCUIT ANALYSIS**
**(Common to ECE, EIE, ETM)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

**PART- A** **(25 Marks)**

1.a) Why is a CE amplifier widely used? List down its main limitations. [2]
b) What are the typical values of h-parameters of CE configuration? [3]
c) What is $f_T$ of a BJT? [2]
d) State Miller's theorem. [3]
e) Compare Frequency stability of crystal oscillator, RC and LC oscillators. [2]
f) What are the advantages of negative feedback? [3]
g) What is Class-A power amplifier? [2]
h) Classify power Amplifiers. [3]
i) What is effect of cascading on single tuned amplifier? [2]
j) What is stagger tuned amplifier? [3]

**PART-B** **(50 Marks)**

2.a) Draw the CE amplifier with un bypassed emitter resistance and derive expression for $R_i$ and $A_v$.
b) A transistor in CB circuit has the following set of 'h' parameters. $h_{ib}$ = 20, $h_{fb}$ = 0.98, $h_{rb} = 3\times10^{-4}$, $h_{ob} = 0.5\times10^{-6}$. Find the values if $R_i$, $R_o$, $A_i$ and $A_v$, if $R_s = 600\Omega$ and $R_L = 1.5\ k\Omega$. [5+5]

**OR**

3.a) Draw the Darlington circuit and derive the expressions for the overall current gain, voltage gain, input impedance and output impedance.
b) With the help of a neat circuit diagram describe the working of a cascade amplifier. [5+5]

4.a) Draw the hybrid-Π model of common emitter configuration and describe each component in the Π-model.
b) Derive the equation for voltage gain bandwidth product for CE amplifier. [5+5]

**OR**

5.a) Discuss the effect of different types of loads to a common source MOS amplifier.
b) Draw the CS FET amplifier equivalent circuit looking into the drain and find its gain and output impedance. [5+5]

6.a) Explain the principle of negative feedback in amplifiers. Show quantitatively the effect of negative feedback on (i) Gain (ii) Stability (iii) Noise (iv) Distortion.

b) Show that current–series negative feedback increases the input impedance and increases the output impedance. [5+5]

**OR**

7. Starting from the description of a generalized Oscillator, derive the expression for frequency of Oscillation in a Colpitts Oscillator. [10]

8. Describe the operation of Class B Push pull amplifier and show how even harmonics are eliminated. [10]

**OR**

9.a) Derive the expression for maximum conversion efficiency for a simple series fed Class A power amplifier.

b) A push pull amplifier utilizes a transformer whose primary has a total of 160 turns and whose secondary has 40 turns. It must be capable of delivering 40W to an 8 Ω load under maximum power conditions. What is the minimum possible value of $V_{cc}$? [5+5]

10. Explain the operation of doubled-tuned amplifier with a neat circuit diagram and derive the equation for its gain bandwidth product. [10]

**OR**

11. What is the effect of cascading double tuned Amplifiers on Band width? Derive the related equations. [10]

**---ooOoo---**

**Code No: 124CV** **R15**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, December - 2017**
**ELECTRONIC CIRCUIT ANALYSIS**
**(Common to ECE, EIE, ETM)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

## PART- A

**(25 Marks)**

1.a) Draw a small signal low frequency model of a transistor. [2]
b) State dual of Miller's theorem and also write its applications. [3]
c) What is unity crossover frequency? [2]
d) Define a short circuit gain of a transistor in CE configuration at high frequencies. [3]
e) What is effect of negative feedback on amplifier gain? [2]
f) State Barkhausen criterion of oscillator. [3]
g) Why heat sinks are needed? [2]
h) What is mean by crossover distortion? [3]
i) Define Q factor of tuned amplifier. [2]
j) What are the limitations of Single tuned amplifier? [3]

## PART-B

**(50 Marks)**

2.a) The h parameters of a transistor used in single stage amplifier circuit are $h_{ic}$ = 1100, $h_{rc}$ =1, $h_{fc}$==51 and $h_{oc}$=25μA. Determine the amplifier parameters for CC configuration when $R_S$=$R_L$=10K.
b) For any single-stage amplifier express input resistance in terms of current gain and h-parameters only. [5+5]

**OR**

3.a) Derive the bandwidth of a multistage amplifier, assuming that each stage has same upper and lower cut off frequencies.
b) For the two stage amplifier of the figure 1, calculate the input and output impedance, and the individual and overall voltage gains. Assume $h_{fe}$ =50, $h_{ie}$=1.1kΩ, $h_{re}$ = $h_{oe}$= 0. [5+5]

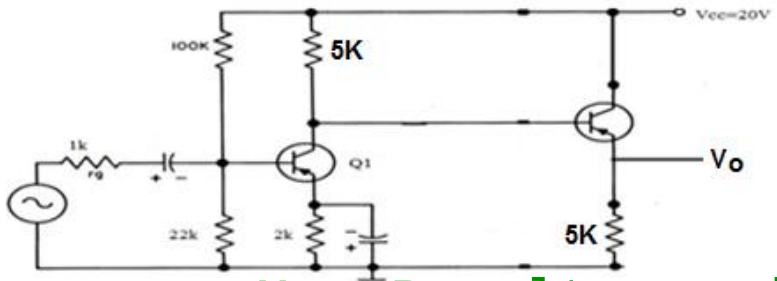





**Figure: 1**

4.a) A transistor biased at 20mA, 20V, it has the h-parameters at room temperature $h_{ie}$ =500Ω, $h_{fe}$=100, $h_{re}$ =$10^{-4}$, $h_{oe}$ =$4\times10^{-5}$℧. It has $f_T$ =50MHz and $C_C$=3pF. Find all the values of hybrid π components.

b) The 3-db bandwidth of an amplifier extends from 20 Hz to 20 kHz. Find the frequency range over which the voltage gain differs by only 1 dB from the mid band value. [5+5]

**OR**

5.a) The amplifier of figure 2 uses a FET with $I_{DSS}$ =3mA, $V_p$= -3V, $r_d$>>$R_d$. Find the quiescent drain current, quiescent drain to source voltage and $A_V$.

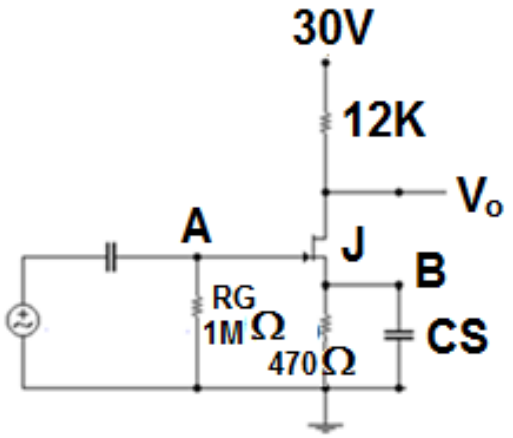



**Figure: 2**

b) Derive the equation for voltage gain of a CS FET amplifier. [5+5]

6.a) An amplifier has an open loop voltage gain of 1000 and delivers 10W output with 10% second harmonic distortion when the input is 10mV. Find the distortion of 60dB of negative feedback is applied.

b) Calculate $A_{vf}$ = $V_0/V_s$, $R_{if}$ and $R_{of}$ for the circuit shown in figure 3 use typical h parameter values. Rs=$R_C$=10K and Re=1K. [5+5]

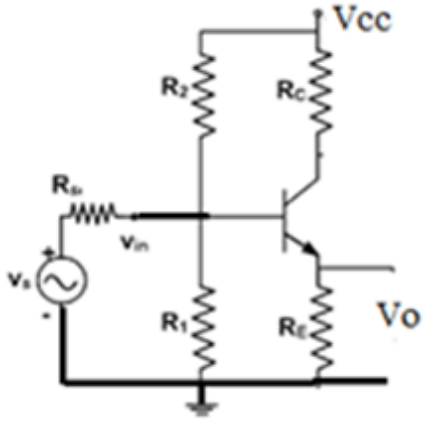



**Figure: 3**

**OR**

7.a) Derive an expression for frequency of oscillations of a RC phase shift oscillator using transistor.

b) A colpitts oscillator is designed with $C_1$ = 100pF and $C_2$=7500pF. Find the range of inductance values if the frequency of oscillations vary between 950 and 2050KHz. [5+5]

8.a) Classify amplifiers based on operating point selection. Compare them in terms of efficiency and distortion.

b) A transformer coupled class A large signal amplifier has maximum and minimum values of collector-to-emitter voltage of 25V and 2.5V. Determine its collector efficiency. [5+5]

**OR**

9.a) What is push pull configuration and how does this circuit reduce the harmonic distortion?

b) Given an ideal class B Push Pull amplifier whose collector supply voltage is $V_{cc}$, and $R_L' = n^2R_L$ are fixed as base current excitation is varied, show that the collector dissipation $P_c$ is zero at no signal, rises as $V_m$ increases and passes through a maximum at $V_m=2V_{cc}/\pi$. [5+5]

10. Draw the circuit diagram of double tuned amplifier and explain its working and derive the equation for bandwidth. [10]

**OR**

11.a) How to reduce the instability in tuned amplifier? Explain them with neat circuit diagram.

b) What are the advantages of stagger tuned amplifier? Draw its frequency response. [5+5]

**---ooOoo---**

**Code No: 124CV** **R15**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, December - 2018**
**ELECTRONIC CIRCUIT ANALYSIS**
**(Common to ECE, EIE, ETM)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

## PART- A

**(25 Marks)**

1.a) How the amplifiers are classified? [2]
b) State and prove Miller's theorem. [3]
c) What is gain bandwidth product? [2]
d) Why emitter bypass capacitor is needed? [3]
e) How the stability of amplifier will affect by negative feedback amplifier? [2]
f) State the necessary conditions for oscillator. [3]
g) Define conversion efficiency of power amplifiers. [2]
h) How is crossover distortion eliminated in class AB amplifier? [3]
i) What are the applications of tuned amplifier? [2]
j) What is the coefficient coupling in a double tuned amplifier? [3]

## PART-B

**(50 Marks)**

2.a) Draw the equivalent circuit for the CE and CC configurations subject to the restriction that $R_L = 0$. Show that the input impedance of the two circuits are identical.
b) The transistor amplifier shown in figure 1 uses a transistor with typical h parameter values. Calculate $A_i$, $A_V$, $A_{Vs}$, $R_o$ and $R_i$. [5+5]

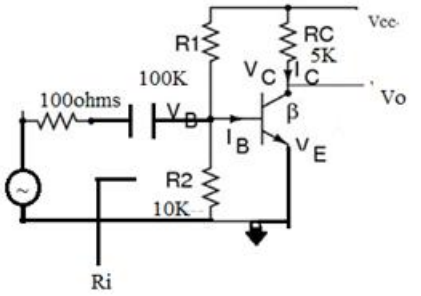



**Figure: 1**

**OR**

3.a) Draw the circuit diagram of Darlington emitter follower and derive the expression for input impedance.
b) Explain the working of cascade amplifier with neat circuit diagram. [5+5]

4.a) Draw the hybrid π equivalent circuit of a transistor in CE configuration and explain the various parameters in it.

b) A transistor biased at 5mA, 10V, $h_{ie}$ =600Ω, $h_{fe}$=100, $C_C$=3pF and current gain of 10 at a frequency of 20MHz. Find β cut off frequency, gain band width product, $C_e$, $r_{b'e}$ and $r_{bb'}$ [5+5]

**OR**

5.a) Calculate the voltage gain of the FET amplifier shown in the figure 2. Assuming blocking capacitor to be large.$g_m$=4mA/V and $r_d$ =5K.

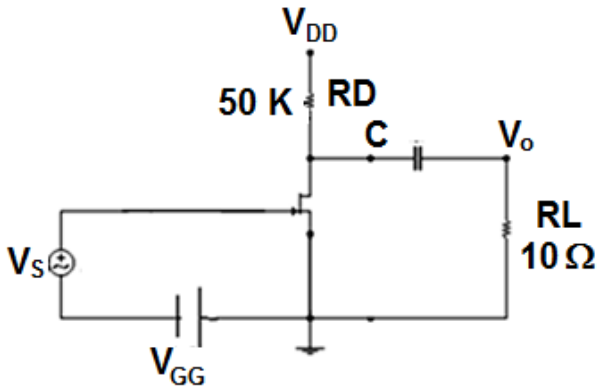



**Figure: 2**

b) Sketch the small signal model of a CD FET amplifier and derive equation for the voltage gain. [5+5]

6.a) Draw the negative feedback topologies and explain them.

b) An open loop amplifier has a midband gain of 500 and a pass band from 50Hz to 50KHz. Find voltage gain and cut off frequencies if 10% of output voltage is fed back. [5+5]

**OR**

7. Derive an expression for frequency of oscillations of a wien bridge oscillator using transistor. [10]

8.a) Explain how the efficiency of the class A power amplifier is improved by the transformer coupled amplifier configuration?

b) A transformer coupled class A power amplifier supplies the power to an 80Ω load connected across the secondary of a transformer having turns ration of 5:1. If $I_c$ =120mA, find maximum output power? [6+4]

**OR**

9.a) Derive an equation of output power of a class B power amplifer.

b) Draw the circuit diagram of complementary symmetry class B pushpull amplifier and explain its working. [5+5]

10.a) Why is double tuning employed in tuned amplifier? What are the advantages of it?

b) What are applications of stagger tuned amplifier? [5+5]

**OR**

11.a) What are the high frequency limitations of a tuned amplifier? How are they eliminated?

b) How is the bandwidth of tuned amplifier improved? Draw such a circuit and explain its working. [5+5]

**---ooOoo---**

**Code No: 154AW** **R18**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B. Tech II Year II Semester Examinations, November/December - 2020**
**ELECTRONIC CIRCUIT ANALYSIS**
**(Common to ECE, EIE)**

**Time: 2 Hours** **Max. Marks: 75**

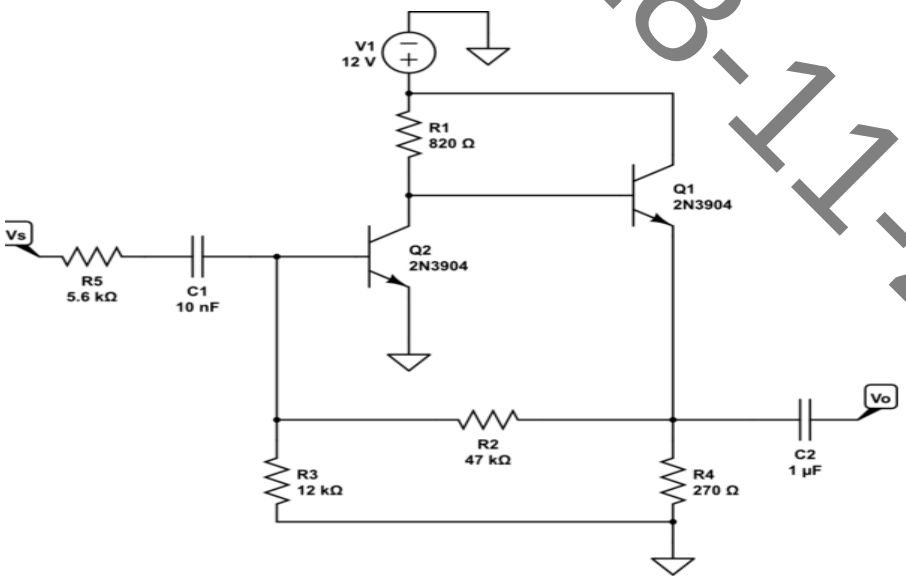
**Answer any Five Questions**
**All Questions Carry Equal Marks**
- - -

1.a) Derive the upper and lower cutoff frequencies of the common emitter amplifier.
b) Why 3dB frequency for the current gain is not same as the 3dB frequency for voltage gain? [9+6]

2.a) The bandwidth of a single stage amplifier extends from 10Hz to 100kHz. Find the frequencies at which the voltage gain is down by 1dB from its mid-band value.
b) Draw the circuit diagram of Darlington pair and explain how it provides high input impedance. [6+9]

3.a) A voltage amplifier is characterized by an open loop voltage gain of 100. Input resistance of 50KΩ and output resistance of 2KΩ, Negative feedback of 10% of output voltage is introduced in series with the input to bring the distortion below acceptable level. Find the modified values of these parameters.
b) Draw the current shunt feedback circuit diagram. [8+7]

4. Determine the feedback factor, current gain, voltage gain, input and output impedances for the following circuit. Assume ideal h parameters for the transistors. [15]




5. Derive the expression for the phase shift as a function of frequency for the feedback network of RC phase shift oscillator. [15]

6.a) How does the frequency stability of an LC oscillator depend upon the Q-factor of the LC circuit? Explain.

b) Determine the minimum amplifier gain and the phase shift required to be introduced by the amplifier for the following case: Feedback factor =2%, oscillator type is Hartley oscillator. [8+7]

7.a) A class B amplifier provides a 15V peak output signal to 10Ω load. The system operates on a power supply of 20V. Determine the efficiency of the amplifier.

b) Draw the circuit diagram of push-pull class-B power amplifier and explain its working. [7+8]

8.a) Define the terms slope error, displacement error, transmission error.

b) With the help of circuit diagram explain the principle of operation of a constant current sweep circuit. [7+8]

**---ooOoo---**

**Code No: 114DN** **R13**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, October/November - 2016**
**PULSE AND DIGITAL CIRCUITS**
**(Common to ECE, ETM)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

**PART - A** **(25 Marks)**

| | | |
|---|---|---|
| 1.a) | What do you mean by linear network? | [2] |
| b) | Why RC circuits are commonly used compared to RL circuits. | [3] |
| c) | Distinguish between comparators and clipping circuits. | [2] |
| d) | What do you mean by double ended clipper? | [3] |
| e) | How does diode acts as a switch? | [2] |
| f) | What do you mean by turn ON time of a transistor? | [3] |
| g) | What are the applications of Schmitt trigger? | [2] |
| h) | What are the applications of time-base generators? | [3] |
| i) | What do you mean by synchronization? | [2] |
| j) | Name the technologies which use bipolar transistors. | [3] |

**PART - B** **(50 Marks)**

2.a) Prove that for any periodic input waveform the average level of the steady state output signal from the RC high pass circuit is always zero.
b) Derive an expression for the rise time of the output of a low pass RC circuit excited by a step input. [5+5]

**OR**

3.a) Prove that a low pass RC circuit with a large time constant acts as an integrator.
b) Derive the expression for percentage tilt of a square wave output of RC high pass circuit. [5+5]

4.a) Draw the basic circuit diagram of negative peak clamper circuit and explain its operation.
b) With help of a neat circuit diagram explain the working of a two – level diode clipper. [5+5]

**OR**

5.a) State and prove clamping circuit theorem.
b) Write short notes on transistor clippers. [5+5]

6.a) Explain the operation of transistor switch in saturation.

b) For a common emitter amplifier, $V_{cc}$ = 15V, $R_c$ = 1.5kΩ and $I_B$ = 0.3 mA. Determine the value of $h_{FE(min)}$ for saturation to occur, if $R_c$ is changed to 500 Ω will the transistor be saturated. [5+5]

**OR**

7.a) With the help of a neat circuit diagram and waveforms, explain the operation of Four diode sampling gate.

b) With the help of a neat circuit diagram and waveforms, explain the operation of Six diode sampling gate. [5+5]

8.a) Explain the operation of fixed-bias binary with a triggering circuit and waveforms.

b) Design a Schmitt trigger circuit to have UTP=6V and LTP=3V using silicon Transistor Whose $h_{FE(min)}$=40. Assume necessary data. [5+5]

**OR**

9.a) Draw the circuit diagram of Bootstrap time base generator and explain its operation with necessary waveforms.

b) Compare the voltage and current time base generators with some examples. [5+5]

10.a) Illustrate the terms synchronization and frequency division of a sweep generator.

b) With the help of neat waveforms explain sine wave frequency division with a sweep circuit. [5+5]

**OR**

11.a) With a neat circuit diagram explain the operation of a TTL tristate output.

b) With the help of neat circuit diagram and truth table explain

(i) RTL OR gate

(ii) RTL AND gate. [5+5]

**Code No: 114DN** **R13**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, May - 2015**
**PULSE AND DIGITAL CIRCUITS**
**(Common to ECE, BME)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

**Part- A** **(25 Marks)**

| | | |
|---|---|---|
| 1.a) | Define rise time. | [2M] |
| b) | Draw and briefly explain the RC differentiator circuit. | [3M] |
| c) | What is meant by clipping in wave shaping? | [2M] |
| d) | Explain Clipping at two independent levels with circuit. | [3M] |
| e) | Compare unidirectional and bi-directional Sampling Gates. | [2M] |
| f) | Draw the Piecewise Linear Diode Characteristics. | [3M] |
| g) | Write a basic principle of time base generator. | [2M] |
| h) | Write the Methods of Generating Time Base Waveform. | [3M] |
| i) | Define positive and negative logic systems. | [2M] |
| j) | List out the applications of sweep circuits. | [3M] |

**Part-B** **(50 Marks)**

2. Draw the output of the low pass RC circuit for different time constant to
a) Pulse input.
b) Step voltage input. [5+5]

**OR**

3.a) Prove that for any periodic input waveform the average level of the steady state output signal from RC high pass circuit is always zero.
b) Draw and explain the response of RLC circuit for step input. [5+5]

4. Classify different types of clipper circuits. Draw their circuits and explain their operation and also transfer characteristics. [10]

**OR**

5.a) State and prove clamping circuit theorem.
b) Explain negative peak clipper with and without reference voltage. [5+5]

6.a) Explain the operation of linear bidirectional sampling gate using transistors.
b) Explain in detail the junction diode switching times. [5+5]

**OR**

7.a) Explain about basic operation principles of sampling gates.
b) Write the advantages and disadvantages of unidirectional diode gate. [5+5]

8. Explain with neat diagram the following methods of linearizing a voltage sweep.
   a) Miller Sweep
   b) Bootstrap weep.
   Compare their merits and limitations. [5+5]

**OR**

9. Draw and explain the working principle of bistable multivibrator circuit and also explain the merits and limitations of it. [10]

10.a) Explain about DTL NAND gate.
   b) Distinguish between voltage and current sweep circuit. [4+6]

**OR**

11. Draw the circuit of a linear current sweep and explain its operation with wave forms. Explain the necessity of generating trapezoidal wave form. [10]

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Code No: 114DN

**R13**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, May - 2017**
**PULSE AND DIGITAL CIRCUITS**
**(Common to ECE, ETM)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

## PART- A

**(25 Marks)**

1.a) Obtain the response of high pass RC circuit for a ramp input. [2]
b) Define % tilt of RC circuit. [3]
c) Write the applications of voltage comparator. [2]
d) Draw Negative biased Negative clipper circuit. [3]
e) Draw the piecewise linear diode characteristics. [2]
f) When transistor acts as a switch? [3]
g) Define multivibrator. [2]
h) Compare different multivibrators. [3]
i) Explain the frequency division in the sweep circuit. [2]
j) Define positive and negative logic systems. [3]

## PART-B

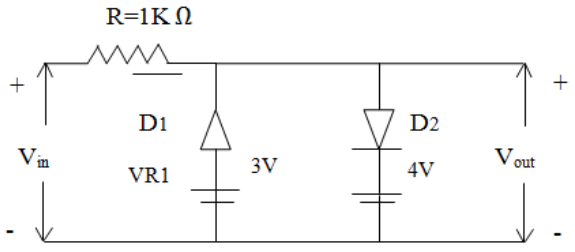
**(50 Marks)**

2. Draw the output of the low pass RC circuit for different time constant to:
a) Pulse input b) Step input. [10]

**OR**

3.a) Derive the expression for percentage tilt for a square wave output of RC high pass circuit.
b) A symmetrical square wave whose peak to peak amplitude is 2μ and whose average value in zero is applied to an RC integrator circuit. The time constant is equal to half the period of square wave, find the peak to peak value of output amplitude. [6+4]

4.a) Draw the circuit diagram of a DC restorer circuit with and without reference voltage and explain its operation for a sinusoidal input signal.
b) Explain the operation of the following double diode clipper and sketch the output wave form for a sinusoidal input shown in figure. [5+5]




**OR**

5.a) State and prove clamping circuit theorem.
b) Explain negative peak clipper with and without reference voltage. [5+5]

6.a) Explain the operation of linear bidirectional sampling gate using transistor.

b) Explain in detail the junction diode switching times. [6+4]

**OR**

7.a) Explain with relevant diagram the various transistor switching times.

b) For a CE circuit $V_{CC}$ = 10V, $R_C$= 1K Ω IB =0.2A. Determine

i) The value of $h_{fe(min)}$ for saturation to occur.

ii) If $R_C$ is change to 220Ω, will the transistor be saturated? [5+5]

8.a) Draw the circuit of a self biased transistor binary and develop the design and steps of analysis.

b) For a mono stable vibrator calculate the input pulse width for the design values of $R_C$ = 2k Ω $R_B$ = 10K Ω C = 0.1 μ F, $V_{CC}$ = 10V and $V_{BE}$(Sat) = 0.8V. [5+5]

**OR**

9. Draw and explain the working principle of astable multivibrator circuit and also explain the merits and limitations of it. And also derive the expression for its pulse width. [10]

10. Discuss in detail the sine wave frequency division with a sweep circuit. [10]

**OR**

11. Draw and explain 2-input NAND gate with functional table. [10]

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**Code No: 114DN** **R13**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech II Year II Semester Examinations, May - 2016**
**PULSE AND DIGITAL CIRCUITS**
**(Common to ECE, ETM)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART - A** **(25 Marks)**

1.a) Why does resistive attenuator need to be compensated. [2]
b) Derive an expression for the output of a high-pass circuit excited by a ramp input. [3]
c) Draw the basic circuit diagram of negative peak clamper circuit. [2]
d) Explain the working of an emitter coupled clipper. [3]
e) Explain the effect of pedestal in gate circuit. [2]
f) Explain the variation of saturation parameters of transistor with temperature? [3]
g) Define UTP and LTP. [2]
h) Write the difference between current time base generator and voltage time base generators. [3]
i) Draw the diagram of OR gate using diodes. [2]
j) Explain the principle of synchronization. [3]

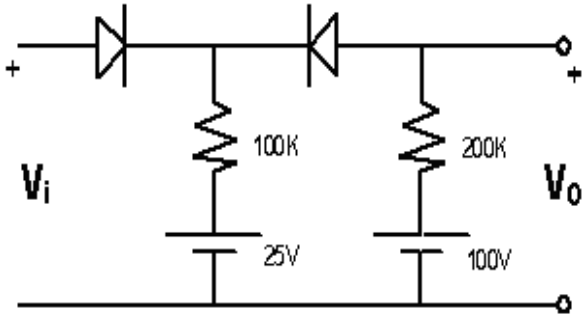
**PART - B** **(50 Marks)**

2.a) A symmetrical square wave whose peak-to-peak amplitude is 8V and whose average value is zero is applied to an RC integrating circuit. The time constant is equal to half -period of the square wave. Find the peak to peak value of the output amplitude.
b) Explain the working of high-pass RC circuit as a differentiator. [5+5]

**OR**

3.a) Derive the expression for rise time of integrating circuit and prove that it is proportional to time constant and inversely proportional to upper 3 dB frequency.
b) Draw the response of the circuit for step input critically damped and over damped cases for a fixed value of R and C. [5+5]

4.a) For the circuit shown in figure, an input voltage $V_i$ linearly varies from 0 to 120 V is applied. Sketch the output voltage $V_o$ to the same time scale. (Assume ideal diodes).




b) State and prove the clamping circuit theorem. [5+5]

**OR**

5.a) Classify different types of clipper circuits. Give their circuits and explain their operation with the aid of transfer characteristics.

b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation. [7+3]

6.a) Write a short note on switching times of a transistor.

b) With the neat circuit diagram, explain the operation of unidirectional sampling gate for multiple inputs. [5+5]

**OR**

7.a) Discuss in detail about breakdown voltages of a transistor.

b) Illustrate the errors encountered in series sampling and what is the design procedure to minimize these errors? [5+5]

8.a) With the help of neat circuit diagram and waveform, explain the principle of operation of collector coupled monostable multivibrator.

b) Explain how the deviation from linearity is expressed in terms of errors. [6+4]

**OR**

9.a) With the help of a neat circuit diagram and waveforms, explain the working of a transistor bootstrap time base generator.

b) What is hysteresis? Explain how hysteresis can be eliminated in a Schmitt trigger? [6+4]

10.a) Explain working of monostable relaxation device as a divider.

b) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL NAND gate with this. [5+5]

**OR**

11.a) What is phase jitter? How to reduce it in frequency division?

b) Draw and explain a diode AND circuit for negative logic and how it works. And how an OR circuit acts as a buffer circuit? [5+5]

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